A Survey of Multilevel Inverter based on Cascaded H-Bridge Topology and Control Schemes

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Abstract

In this study, a review of cascaded H-bridge multilevel inverter topology and control schemes was conducted. Multilevel inverter topology (MLI) H-bridge cascade is implemented to reduce harmonic for high power applications. Applications of multilevel converters are able to reduce the number of harmonics contained in the system of low-voltage electrical distribution. Each topology has their own advantages and disadvantages. The cascaded H-bridge multilevel inverter topology requires only a single DC power source with both input and output, high availability, and the control of power flow in the regenerative version. The selected switching technique to control the inverter will also have an effective role on harmonic elimination while generating the ideal output voltage. Intensive studies have been performed on carrier-based, sinusoidal, space vector and sigma delta PWM methods in open loop control of inverters. The results from this study represent a beneficial basis for matching of inverter topology and the best control scheme according to different application areas.

Keywords: SPWM, Multilevel inverter (MLI), PWM.

1. Introduction

In general, increasing the switching frequency in voltage source inverters (VSIs) leads to better output voltage and current waveforms [1]. Harmonic reduction in controlling a VSI with variable amplitude and frequency of the output voltage is important, and thus, conventional inverters which are referred as two-level inverters require increased switching frequency along with various PWM switching strategies [2]. The multilevel fundamental switching scheme is used to control the needed power electronics switches. Also, a method is presented where switching angles are computed such that a desired fundamental sinusoidal voltage is produced and at the same time certain higher order harmonics are eliminated [3]. The generalized multilevel inverter topology can balance each voltage level by itself regardless of the inverter control and load characteristics. The concept of multilevel converters has been introduced since 1975. The usage of these applications has become more diverse and affects a wide field of electrical engineering from a few watts to several hundred megawatts [4], [5]. Converting static structures that comprise mainly applications of power electronics is becoming increasingly powerful, and the technology has had to adapt to the growth of the power to convert [6]. Multilevel inverter topologies are the Neutral-Point Clamped (NPC) inverters (or Diode-Clamped inverters), the cascaded H- bridge inverters (CHB), and the Flying Capacitor (FC) inverters (or Capacitor Clamped inverters), as shown in Figure 1 [7]. In this paper, a review of multilevel inverter based on cascaded h-bridge topology and control schemes was conducted. The advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability [8]. One of the purposes is to measure the total harmonic

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distortion (THD) [9].

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_1}$$

H1= equals to the fundamental component, where the frequency is *w0* and H_n equals to the n[th] harmonics at frequency nw$_0$

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \quad let\ H_{(n)} = h_n\ and\ H_1 = h_1$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_{(n)}^2}}{h_1}$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{1}{n} \sum_{k=1}^{s} \cos(n\alpha_k)\right)^2}}{\sum_{k=1}^{s} \cos(n\alpha_k)}$$

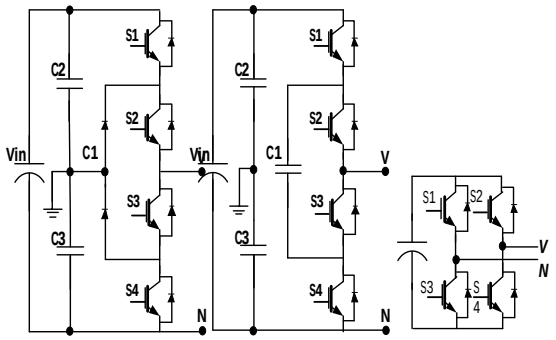

Fig. 1. Topologies of three types of multilevel inverters (three level inverters): (a) NPC-MLI, (b) FC-MLI (c) CHB-MLI [7].

2. Circuit Topology Cascaded H-bridge Multilevel Inverter (CHB-MLI)

Cascaded H-bridge multilevel inverter (CHBMLI) is different in several aspects from NPCMLI and CCMLI on the approach to achieve voltage waveform at several levels. It uses cascaded inverters H-bridge DC-separated sources in the preparation of units, thus creates escalating waveform [10]. In Fig 2, there is only one way to eliminate the leg at the five-cascaded H-bridge inverter, and it can be observed that the entire module of H-bridge have units that accumulate to the CHBMLI topology [11]. The H-bridge unit itself is CHBMLI three levels, where each additional unit cascaded to be extended with two levels of voltage inverter. In Fig 2, there are two H-bridge modules to create five variation voltage levels. CHBMLI applications, for example, are suitable with the use of photovoltaic cells, battery or fuel cells [6]. This is an example of that can be used in power electric vehicles with many cells.

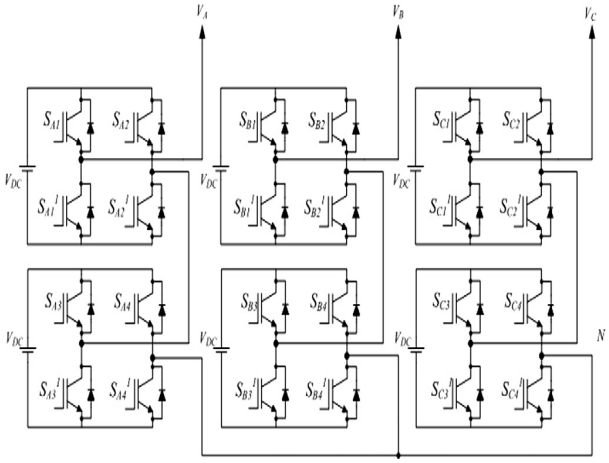

Fig. 2. Three-phase five-level cascaded H-bridge multilevel inverter [10].

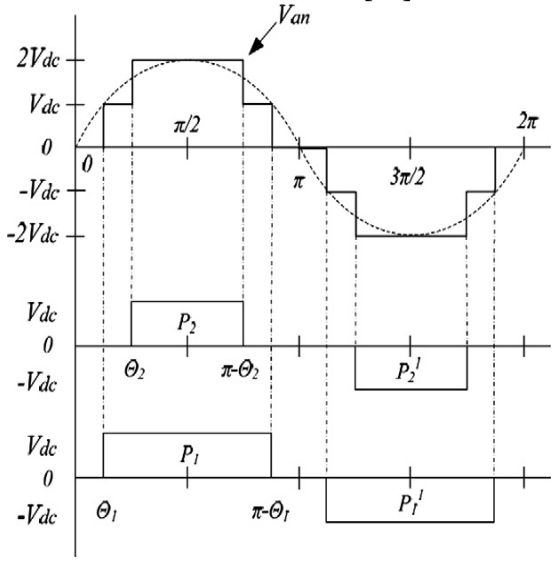

Fig. 3. Phase voltage output waveforms for five-level CHB-MLI with two separate DC sources [12].

The total output voltage in Fig 3 is the sum of the outputs of all units of the full bridge inverter, and all

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H-bridge can create three voltages (+Vdc, 0 and –Vdc) [13]. To change the level of voltage to the output phase, CHBMLI rotates on a switch (one-off) in an H-bridge unit. The unit for voltage H-bridge is added to the VCHB, which are switches S_{A1}, S_{A1}^{1}, S_{A2}, and S_{A2}^{1} as seen in the first cell. Fig 2 show +Vdc, S_{A1} and S_{A2}^{1}switches are turned on, whereas –Vdc, S_{A2} and S_{A2}^{1} are turned off. Complete 0 voltages are obtained by running two buttons on the top half of the full bridge, S_{A1} and S_{A2} switches, or S_{A1}^{1} and S_{A2} switches [14]. n is assumed as the number of modules connected in series, and m is the number of output levels in each phase as seen in Eq. (1). The switching states of a CHB-MLI (sw) can be determined by using Eq. (2).

$$m = 2n+1 \quad (1)$$

$$sw = 3^{m} \quad (2)$$

Output 2*N* +1 is shown in Fig 3, whereby the output voltage wave forms five-level. In order to reduce the total harmonic distortion, the switching angles can be optimized by adjusting them [12].

3. Control Technique for Cascaded H-Bridge Multilevel Inverter

Multilevel inverters achieve high voltage switching through a series of work steps. One of the most important problems in the control of a multilevel inverter is to get a variable amplitude and frequency sinusoidal output using a simple control technique [15]. The first impression of the multilevel converters is that a large number of switching may cause the switch configuration of complex topology. Many techniques are applied to the inverter topology [16], [17]. Control technologies can be divided into multi-PWM inverter technology and selective harmonic elimination sinusoidal PWM (SPWM), space vector PWM (SVM), and similar variations of the three main algorithms as seen in Fig 4. This section presents the methods and reviews some of the basic researches that have been done in this area [18].

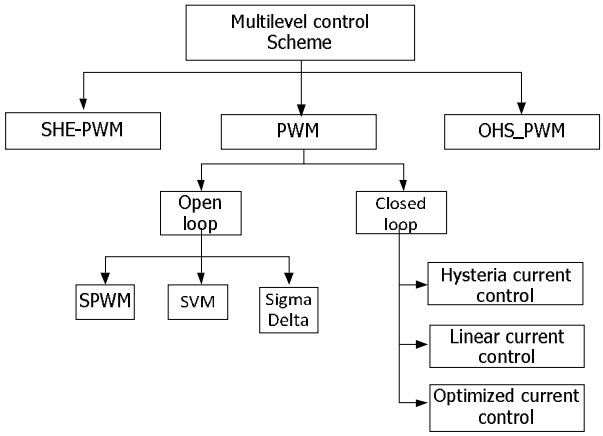

Fig.4. Classification of control schemes of multilevel inverter [17].

A. Sinusoidal Pulse-Width Modulation

The majority of PWM inverters used techniques based on the sampling method. Control technology is the most popular method of pulse width modulation sine adapter's two traditional levels [19]. The term sinusoidal PWM refers to the production of the PWM output signal with a sine wave as a modulation signal. Fig 7 shows the on and off instants of a PWM signal. In this case, it can be determined by comparing the sinusoidal signal (wave modulation) with a triangle wave frequency (carrier wave) as shown in Fig 8. The sinusoidal PWM technology is commonly used in industrial applications and abbreviated here as SPWM [20]. Frequency of the modulating wave determines the frequency of the output voltage. The enlargement of the height of the modulation index of the waveform determines the composition turn control of the RMS value in the output voltage [21]. Fig 5 shows seven-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to neutral was about 194.5 V RMS, and the Modulation Index was equal to 0.95. The value of the THD_V of the voltage was around 5.98%, as shown in Fig 6.

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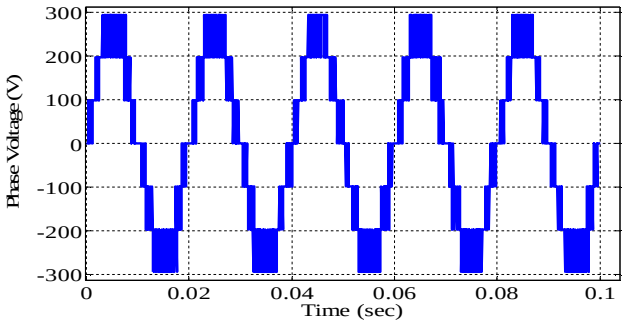

Fig. 5. Phase Voltage at MI=0.95.

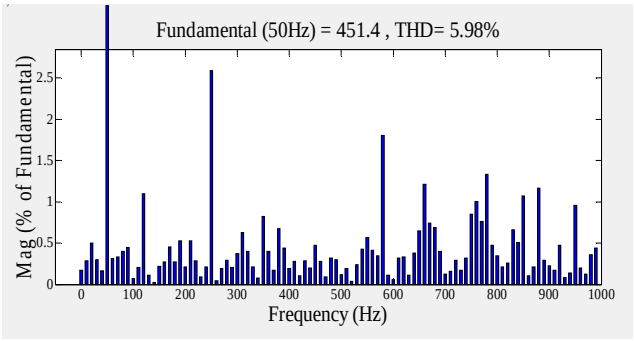

Fig 6. Harmonic Voltage at MI=0.95.

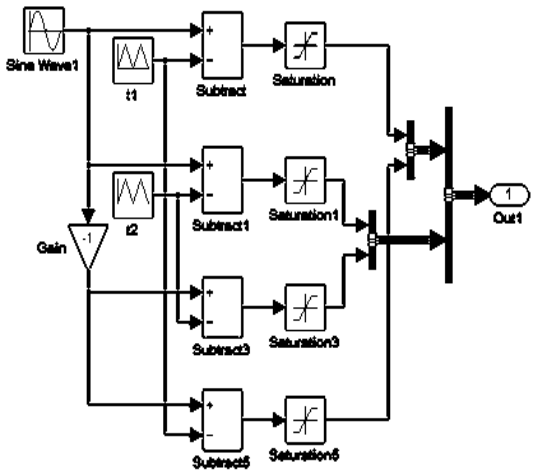

Fig.7. Simulink for Five Level of control signal Cascaded H-Bridge Multilevel inverter.

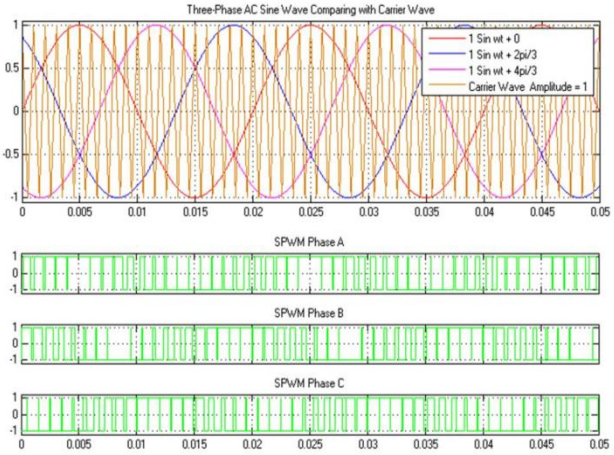

Fig 8. Sinusoidal Pulse Width Modulation for three-phase inverter.

B. Space Vector PWM (SVPWM)

The SVPWM technique is widely used for bi-level PWM converter control, which can be integrated to multilevel inverters [22]. Fig 9 illustrates the different space vectors topologies for the traditional 3, 5, and 7-level converters. These vector diagrams are universal regardless of the topology of multilevel converter. As a result, it can be implemented for diode-clamped, capacitor-clamped, or cascaded converters [23]. The advantages of implementing the Space-vector PWM method are: i. Good utilization of DC-link voltage and low current ripple, and ii. Digital signal processing (DSP) can be interfaced and executed easily [24]. Moreover, there is less complexity in using the control system. A conceptually different control method for multilevel converters, based on the space-vector theory, has been introduced, which is known as space vector control (SVC) [1].

(a) (b)

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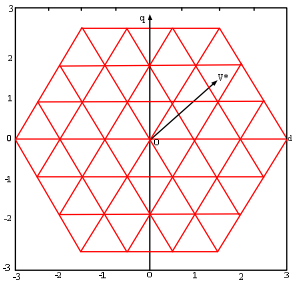

(c)

Fig 9: Space vector diagram (a) three-level; (b) five-level; (c) seven-level [1].

C. Selective harmonic elimination for multilevel inverter

Since the advent of the new family of semiconductors, there has been a strong interest in inverter technology. The ability of switching turn-off times in the range of a few microseconds has increased the flexibility of achieving a practically sinusoidal output by employing sophisticated switching patterns in inverter circuits. Harmonic elimination or the term 'to eliminate harmonic' refers to the set option (programme) of switching angles designed to eliminate specific harmonics [26]. Selective Harmonic Elimination PWM was first introduced in 1970s [27]. The method effectively eliminates some harmonics that are randomly selected by switching the DC link voltage conversion, turning on and off via power switches on certain predetermined points [28]. Selective harmonic elimination has been used in the PWM inverter. By solving the angles of the shift pulse, specific harmonics can be eliminated, depending on the number of harmonics of the elimination pulse available. Furthermore, it has been described as a general structure of a multi-level inverter in 1980s [29][5], as it can be identified by a number of measures, height, and display, either for a particular design to eliminate certain harmonics or to reduce total harmonic distortion. The presented technique synthesizes waveform by the multilevel inverter using cascaded inverter with separate DC sources [30]. This method can eliminate specified order harmonics, minimize the amount of specific order harmonics, and can deal with a wide range of modulation indices, but the THD is not improved compared to the traditional selective harmonics method [31].

3.1 Artificial Intelligence Controller based on Multilevel Inverter Harmonic Filter

The proposed five-levels Cascaded H-bridge inverter (CHB) for harmonic filter has filter and Artificial Intelligence (AI) based on control [32].

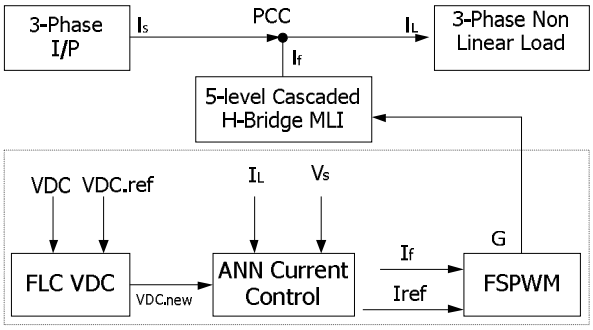

Fig. 10. Control diagram of Artificial Intelligence (AI) for multilevel harmonic filter.

The proposed scheme is compared with two level filter to achieve better compensation as shown in Figure 8. The performance by using smaller filter inductors reduced switching of higher frequency stress and higher voltage [24][33]. However, filters based on MLIs are generally more costly and more complex to control as the filters have higher number of switching inverter states. Furthermore, the application of these filters in medium and high voltage with high power level is justified in terms of cost and performance. In the proposed scheme, power theory is modified and the compensating component is extracted using Artificial Neural Network (ANN) [34]. Moreover, the scheme uses two separate Fuzzy Logic Controllers (FLC), one is for regulating DC voltage and another for generating gate pulses for IGBT in the multilevel inverter as shown in Fig 10 [16].

A. Artificial neural network

The proposed control current of the reference signal is acquired by using the ANN based on instantaneous power (p–q) theory (IPT) developed by Akagi in 1982. The Clarke/Inverse Clarke transformation is based on time domain. The IPT is practical and more effective as it can be applied to balanced and unbalanced systems to compare with other procedure under either steady state or transient

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condition [35]. In this proposal scheme, ANN is used to extract harmonic reduction. For the projected control, only average constant component is desirable, and those undesirable are eliminated. Traditionally, the separation of harmonic component uses a low pass filter, which requires tuning for changes in system. ANN is used to eliminate the repeated tuning and is self-adjusting according to the difference parameter system [36].

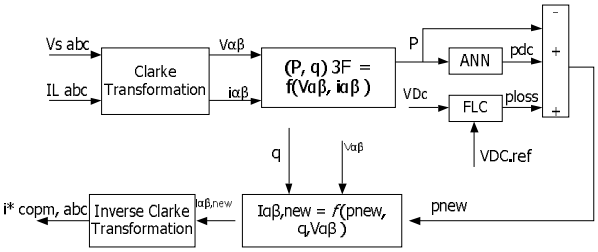

Fig 11. Artificial Intelligence (AI) based on Instantaneous power theory [36].

ANN with the harmonic component from active part is calculated as shown in Fig 11. The fuzzy logic controlled DC voltage is also calculated, and P_{loss} is determined for reference estimation in cohesion with harmonic components to be eliminated. This component comprises the control circuit of the harmonic filter [37].

B. Fuzzy Logic Controller (FLC)

The idea of fuzzy logic controller introduced by Prof. Zadeh in 1965 has become popular recently [26]. The Fuzzy Logic Controller (FLC) uses partial assembly similar to human thinking function rather than using crisp membership function. According to Fig 12, the procedure of basic controllers design is same for both; however, the characteristic features are exclusively described for each controller [38]. The design of fundamental steps follows the input and output parameters. There is a variety of assembly functions and modelling of control rules. There are also possible inferences from assembly functions and control rules. Performance tuning of the input and output profit for the desired approach can be found in [29][39].

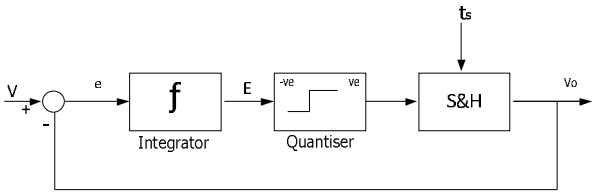

Fig. 12. Block diagrams of delta modulation.

4. Harmonic Elimination of Cascaded H-Bridge Multilevel Inverter

Multilevel inverter works better compared to the conventional pulse width modulation (PWM) inverters. It provides even voltage sharing, both dynamically and statically; as well as reduce the size and harmonic distortion of volume due to the elimination of bulky coupling inductors or transformers [30][40].

The proposed method using ANFIS technique for harmonic elimination can generate the controlling pulses of the electronic power switches, IGBT (Insulated Gate Bipolar Transistor). THD is minimized by controlling switching pulses output voltage (V_{out}) in the multilevel inverter since the reduction of THD eliminate the harmonics present in the inverter (V_{out}) and improve the power quality, which are discussed in [41] [9].

The multilevel inverters control of Sinusoidal Pulse Width Modulation (SPWM) technique uses a number of level shifted carrier waves for comparison with the reference phase voltage signals. The multilevel inverter control of Space Vector Pulse Width Modulation (SVPWM) involves mapping of the outer sectors to an inner sub-hexagon sector to determine the switching time duration for different inverter vectors. Then, the switching inverter vectors correspond to the actual sectors that are switched for the time duration calculated from the mapped inner sectors, which has been discussed in [42].

The Newton-Raphson (N-R) method is one of the most widely used methods for root-finding. It can be easily used to find solutions for a system of non-linear equations [43]. This method has been applied in numeric analysis to reduce harmonic distortion. It requires only the first initial value. The N-R method is used to compute the switching angles for the system given by equation (3) [44]. The range of switching angles between 0 and $\pi/2$ produces the desired essential voltage with the 3rd and the 5th

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harmonic components eliminated for a given modulation index of feasible solutions of equation (3), as discussed in [38].

$$\begin{aligned}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)] &= 3m_a \\ [\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3)] &= 0 \\ [\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)] &= 0\end{aligned} \quad (3)$$

Table 1 compares three phase multilevel 2-level and 3-level inverters for THD. This proves that the proposed scheme can reduce the THD, which is an indispensable condition for PV system [45]. The compared results from five-level SVPWM inverter with two-level SVPWM and three-level SVPWM inverter in terms of THD can be found in [46].

Table 1. Total harmonic distortion for the proposed system.

No. of levels	THD (%)
2	16.10
3	9.08
5	5.68

An improved control algorithm is used to generate the reference signals at the inverter output and transfer PV power to the grid. The impedance of the inductor can be defined as:

$$Zs = Rs + jXLs = |Z_s| \angle \theta \quad (4)$$

The control algorithm is provided by a PIC18F452 microcontroller in the digital control unit. A principle scheme of the digital control unit is shown in Fig. 13 [47].

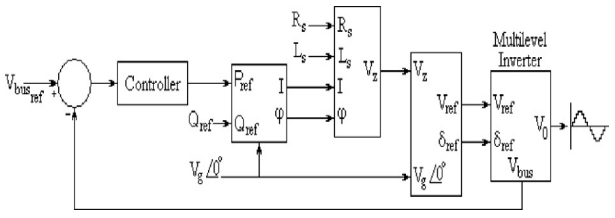

Fig. 13. Proposed Control diagram of PV assisted inverter system.

To ensure the compensation current of APF to trace the reference harmonic and reactive current, an adaptive PI controller is adapted. First, an adaptive closed loop is implemented to detect harmonic and reactive current quickly and robustly as shown in Fig 14 [48].

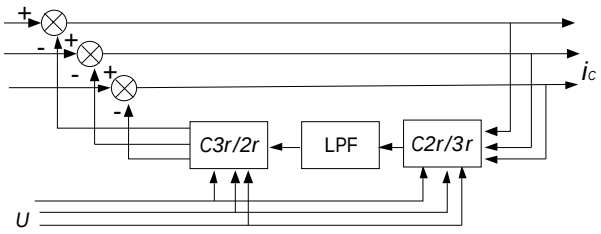

Fig. 14. Harmonic and reactive current detection circuit.

Throughout this work, the control used for different topologies studied is multi-carrier sinusoidal pulse width modulation, whose characteristics are: Sinusoidal PWM; Signal modulating: 50 Hz; Frequency: 2500Hz; Index modulation: 1 [49][50].
The AI controller gives the source current harmonic of 2% for increased RL load and 2.53% for increased RC load during simulation. This controller performs well during experimentation, and also gives 5.6% of harmonic for RL load and 4.8% for RC load for phase [51].
In order to overcome this problem, a fuzzy logic controller is applied and extended to a three-level shunt APF. Fuzzy logic control algorithm is proposed for harmonic current and inverter DC voltage control to improve the performances of the three levels active power filters [52].
The modules and the first H-bridge serve to increase the level of the DC link voltage, and the second H-bridge provides bi-directional power flow through the load [53]. The first Bridge is connected in series with as many modules for every six level increase, with each module intertwined with a switch in series with the source, and the combination shunted through an anti-parallel diode as shown Table 2. The total harmonic distortion (THD) obtained using a harmonic spectrum reveals the mitigation of the frequency components of output voltage as seen in Table 3 [54].

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Table 2.
Comparison in terms of power components used for different level.

No. of levels	No. of power switches		No. of bypass diodes	
	SPSMLDCI	DBMLDCLI	SPSMLDCI	DBMLDCLI
15	10	10	1	2
21	13	11	1	3
27	16	12	1	4
33	19	13	1	5
39	22	14	1	6

Table 3. Comparison chart.

Vo1 (V)	Simulation THD (%)	Hardware THD (%)
100	19.28	21.26
120	15.6	14.36
140	12.8	14.12
160	12.14	13.23
180	9.7	9.12
200	9.67	9.50
220	8.18	7.77

Among these techniques, selective harmonic elimination (SHE) and THD minimization approaches are applied to multilevel inverters in order to eliminate harmonic components of the output voltage [54-52].

CONCLUSION

The choice of cascaded H-bridge (CHB) multilevel inverters should be based on the topology of each inverter used. Each topology has their own advantages and disadvantages. The main advantage of multilevel PWM converters is that the series of connection allows high voltage without increasing the voltage on the effort of switches. The cascaded H-bridge multilevel inverter topology requires only a single DC power source with both input and output, high availability, and the control of power flow in the regenerative version.

This paper has reviewed cascaded H-bridge (CHB) multilevel inverters for recent applications and developments of these inverters, including new proposed topologies, modulation techniques, and control strategies.

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