Design and Implementation of a Bridgeless Zeta Converter for Power Factor Correction in Hybrid Electric Vehicles

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***Abstract*— Hybrid Electric Vehicles (HEVs) integrate an Electric Motor, photovoltaic battery and an IC Engine to achieve better fuel economy qualifying the toxic emissions. They usually need power conditioning circuitry which requires rectification and filtering of input mains power. The rectified output is scaled up/down using DC-DC converter. The filter used at the supply draws current only when the line voltage exceeds the filter capacitor voltage and the filter capacitor is charged to near the peak level of the input line voltage. The current flows for the short duration where the capacitor voltage reaches to peak of input voltage. Due to this short pulses the RMS value of current increases and average value decreases, which adds line losses and power quality issues in the circuit. Hence, an active Power Factor Correction circuit is required to improve power quality. This encompasses a power modulator like an AC – DC converter at the charging end, but the presence of nonlinear devices in the converter topology still induce harmonics and distort the supply current compromising the Power Factor (PF) and Efficiency of the system. Hence, the implementation of a PF Correction (PFC) Circuitry at the charging end of HEVs is of prime importance. Compared to the other topologies in the literature, the Zeta topology is more effective and efficient. Out of the available Zeta Topologies, bridgeless Zeta topology with front end EMI filter is suitable. This paper explores the design and implementation of the bridgeless Isolated Zeta Converter topology as a potential solution to the addressed problems. Performance parameters such as THD (Total Harmonic Distortion) in the supply current, supply pf, energy factor and crest factor will be calculated for the proposed topology. Prototype of the proposed topology for PFC will be built in compliance with the IEC standards to validate the simulation results.**

***Keyword* — Bridgeless Zeta converter, PFC and average current control technique**

I. INTRODUCTION

HEVs entail a power modulator like an AC – DC converter at the charging end of the Photo Voltaic Cell (PVC), but the presence of nonlinear devices in the converter topology induce harmonics and distort the supply current waveform compromising the Power Factor (PF) and Efficiency of the system[1-2]. Hence the harmonic distortion in the supply current has to be checked to the permissible limits. This provides a scope for the design and implementation of an efficient AC – DC Converter topology with inherent Power Factor Correction as shown in Fig.1. Power Factor Correction can be attained by : passive and active methods. But active PFC topologies always draw current in phase and at the same frequency as the line voltage, thereby shaping the input current waveform. Therefore this paper focuses on active power factor correction topologies. The active PFC topology employs a DC-DC boost converter in succession to a conventional diode bridge rectifier (DBR), with the DBR's output fed to the boost converter. Numerous DC-DC converter topologies have been discussed in the literature [3-4]. But this paper depicts about the application of zeta converter for PFC.

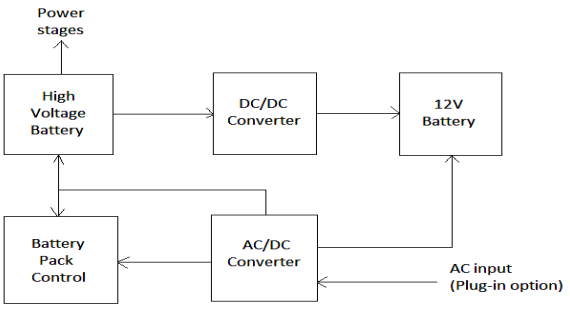

Fig.1Hybrid Electric Vehicle's:charger and converter

The zeta converter proves to be an optimal solution with its desirable characteristics like low voltage ripple, input – output isolation, ability to act like a buck - boost converter[5-6]. The interleaved zeta converter yields a lower

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harmonic distortion than the conventional zeta converter due to the averaging of the inductor ripple by operating two converters in parallel with a time delay of half of the switching period. But, the interleaved zeta converter has a DBR bridge and hence results in higher levels of power losses (Device loss + Conduction loss). This leads to the design of a Bridgeless Isolated Zeta Converter which is discussed in the following sections.

II. BRIDGELESS ISOLATED ZETA PFC CIRCUITRY

A Zeta converter performs a non-inverting buck-boost function. The range of duty ratio is much wider than any other converter. The zeta converter features improved power factor, low input current distortion, low output current ripple and wide output - power range[7]. Moreover, Zeta converter provides

- Input to output DC isolation
- Continuous output current
- Reduced electromagnetic interference (EMI)

Thus, the Zeta converter topology is proposed as the best suited topology in Hybrid Electric Vehicles (HEVs) for Power Factor Correction[8-10]. In this paper, a bridgeless zeta converter is discusses and the circuit diagram is shown in Fig.1.

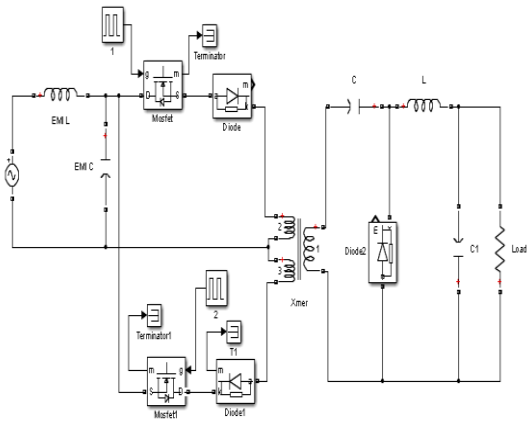

Fig.2 Circuit of Bridgeless Isolated Zeta Converter

(A) WORKING

A Bridgeless Isolated Zeta Topology is designed such that the two switches conduct independently for the positive and negative half cycles of the supply voltage. The conduction losses of the DBR are reduced to half as compared to conventional topology due to the bridgeless configuration. Moreover, it also improves the thermal utilisation of switches since total switch RMS current is divided to two switches. Thus, the operation of the converter can be explained under positive and negative half cycles of supply voltage.

Switch SW_1 and diode D_1 conduct for positive half cycle of the supply voltage and diode D_2 remain reverse biased during this period. Similarly, for the negative half cycle of the supply voltage, switch SW_2 and diode D_2 conduct and no current flows through SW_1 and D_1 as shown in the fig 3.3. The energy is transferred through High Frequency Transformer (HFT) whose turn ratio is N1: N1: N2. The magnetising inductance (L_m) is designed to achieve wide range of DC link control and inherent power factor correction.

Initially, before the positive half cycle of supply voltage, the intermediate capacitor C_1 is charged. During the positive half cycle the switch SW_1 is turned on and the diode D_1 is forward biased. Hence, current flows through SW_1 and diode D_1 and the energy is stored in the HFT and the charge stored in the capacitor C_1 is discharged to the inductor L_o and the DC link capacitor C_d deliver energy to the load.

When the switch SW_1 is turned OFF, the energy stored in the HFT freewheels through the diode D_3. The inductor L_o supplies energy to the load. Thus continuous conduction is obtained at the output for both the switching cycles. During the negative half cycle of the Supply voltage, the same operation is repeated with the switch SW_2 turned on and diode D_2 forward biased. The voltage at the two winding terminals of the primary side of HFT is plotted as follows, for a supply of 24Vrms with a front end EMI filter.

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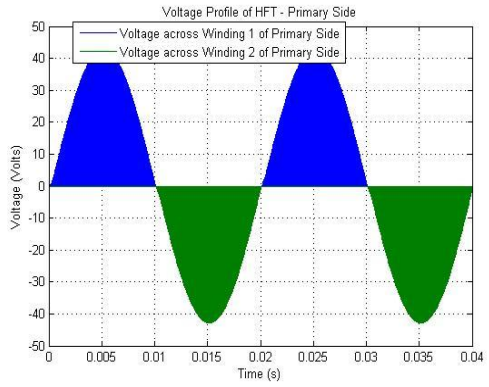

Fig.3 Voltages at the Primary Winding of the HFT

(B) DESIGN EQUATIONS

The Bridgeless Isolated Zeta Converter for PFC is designed as follows: The input voltage V_s is given by [11-12]

$$V_s = V_m \sin(2\pi f_L t) \quad (1)$$

Where V_m is the peak input voltage, f_L is the line frequency. The average input voltage V_{in} is given by,

$$V_{in} = \frac{2V_m}{\pi} \quad (2)$$

The load resistance is given by,

$$R_l = \frac{V_{dc}^2}{P_o} \quad (3)$$

Where, P_o is the output power

The critical value of magnetising inductance Lm of HFT is given by

$$L_{mc} = \frac{R_l(1-D)^2}{2Df_s\left(\frac{N_2}{N_1}\right)^2} \quad (4)$$

Where f_s is the switching frequency,hence the value of magnetising inductance is selected such that

$$L_m << L_{mc}$$

The output inductor L_o is given as,

$$Lo = \frac{V_{dc}(1-D)}{f_s \Delta i_{Lo}} \quad (5)$$

Where i_{LO} is the permitted ripple current in the inductor L_o = 10 % of I_o

The value of intermediate capacitor C_1 is given by

$$C_1 = \frac{V_{dc}D}{\Delta V_{C_{in}} R_l f_s} \quad (6)$$

Where V_{cin} is the permitted ripple voltage in capacitor C_1 = 2 % of V_{dc}

The value of DC link capacitor is given by

$$C_d = \frac{I_{dc}}{2\omega \Delta V_{dc}} \quad (7)$$

Where V_{dc} is the permitted DC link voltage ripple = 2 % of $V_{dc.}$

An EMI filter is designed to avoid the reflection of high switching frequency in the supply system. The filter capacitor C_{max} is designed by,

$$EMI\ C_{max} = \frac{I_{peak} \tan\theta}{\omega_L V_{peak}} \quad (8)$$

Where I_{peak} is the peak input current, V_{peak} is the peak input voltage, θ is the dispacement angle.The value of filter capacitance C_f is selected to be greater than $C_{max.}$

The value of filter inductance L_f is given by,

$$EMI\ L_f = \frac{1}{4\pi^2 f_c^2 C_f} \quad (9)$$

Where f_c is the cut-off frequency = f_s / 10

(C) MATHEMATICAL DESIGN OF THE TOPOLOGY

(i) Specifications

A 75W PFC Bridgeless Isolated Zeta Converter is designed for battery charging in Hybrid Electric Vehicles with the following specifications as shown in Table -1.

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Table:1.Specifications of Isolated Zeta Converter

Specifications	Values
V_s (supply voltage)	24 V
f_L (line frequency)	50 Hz
P_o (output power)	75 W
f_S (switching frequency)	25 kHz
D (duty ratio)	68.95 %
N1:N2 (transformation ratio)	1:1

(D) CALCULATIONS

The design values for the converter with the specifications mentioned in the previous section were calculated using the design equations. Their values have been tabulated and it is shown in table-2.

Table:2. Parameters of Bridgeless Isolated Zeta Converter

Parameters	Values
Load resistance (R_L)	30.7 Ω
Critical value of magnetising inductance (L_m)	25 µH
Output inductor (L_o)	4 mH
Intermediate capacitor (C_1)	1.1 µF
DC link capacitor (C_d)	5 mF
EMI Capacitance (C_f)	2 µF
EMI Inductance (L_f)	2 mH

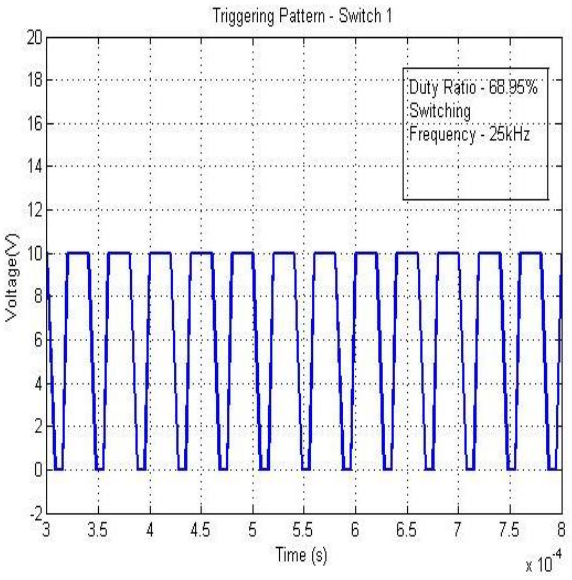

Fig.4 Triggering Pattern for SW_1

The triggering pattern for the MOSFET SW_1 is shown in Fig.4. The switching frequency is 25 kHz with a duty ratio of 68.95%. The second switch SW_2 is triggered with a phase difference of π degrees i.e half of the time period of the triggering pattern. The triggering pattern in MATLAB for the MOSFET SW_2 is as follows,

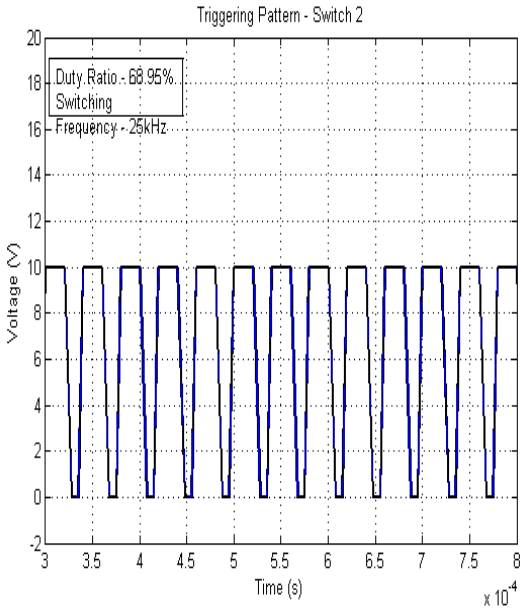

Fig.5 Triggering Pattern for SW_2

The supply current and voltage plots for the circuit are shown in Fig.6.

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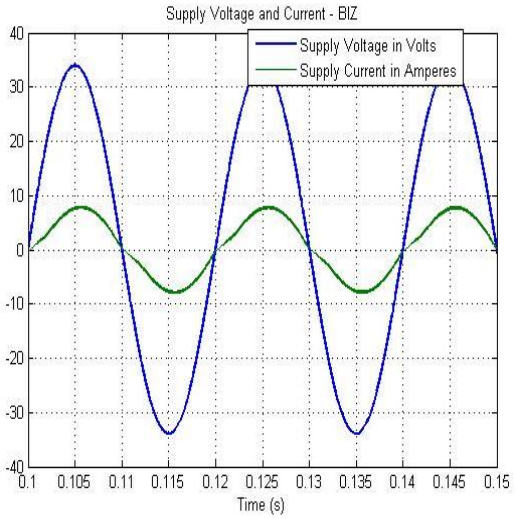

Fig.6 Supply Voltage and Current Waveforms

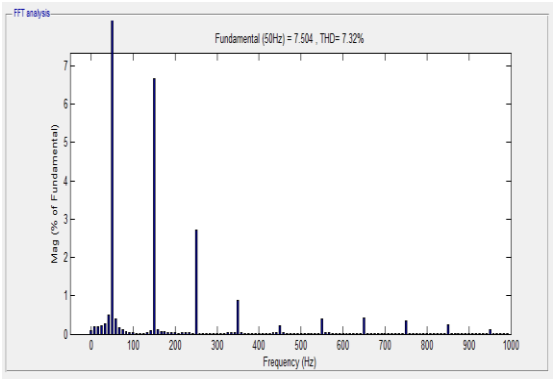

Fig.7 FFT Analysis of the Supply Current

From the FFT analysis shown in Fig.7, the Total Harmonic Distortion (THD) in the supply current was found to be 7.32%.The load voltage plot is as shown in Fig.8 follows,

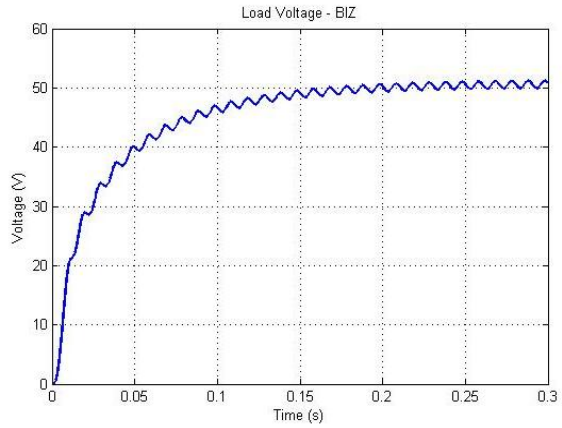

Fig.8 Load Voltage of BIZ Topology

The FFT analysis of the load voltage is as follows(refer Fig.9):

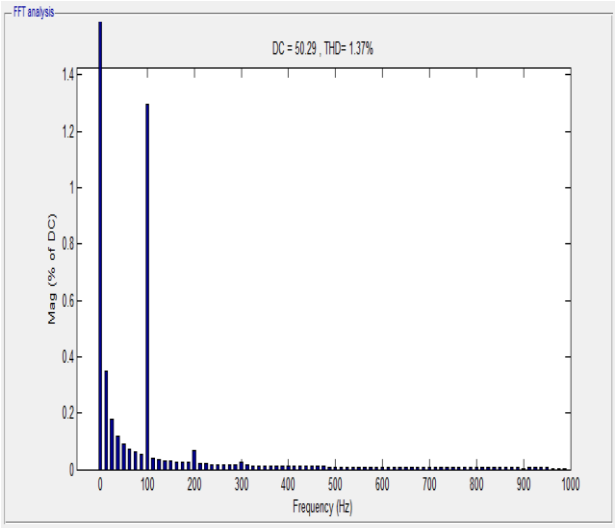

Fig.9 FFT of the Load Voltage

From the above plot, the AC content in the load voltage is less than 2%. This proves that the Zeta topology has lower ripple at the load end.

III. AVERAGE CURRENT CONTROL FOR BRIDGELESS ZETA

The power factor obtained in the open loop configuration of the converter can be enhanced by adopting current control techniques[13-14]. By introducing the feedback and feed forward loops, lower harmonic profile can be maintained. The general control principle of the controller is that the supply current is forced to track a generated sinusoidal reference so that the converter draws a sinusoidal current; thereby power factor is improved. Generally two loops are implemented in the controller; to control the instantaneous input current to follow the same wave shape as the instantaneous input voltage, current feedback loop is implemented. The other loop is a voltage feedback loop which adjusts the input current so as to maintain a constant output voltage as shown in Fig.10. The low-bandwidth outer loop with characteristic $G_L(s)$ is used to keep the output voltage of the PFC stage constant and to provide the error signal V_e. The high-bandwidth inner loop with characteristic $G_H(s)$ is used to control the input current.

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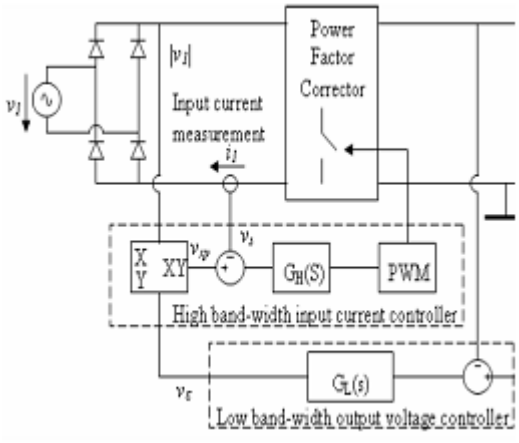

Fig. 10. General control scheme for PFC using a switching converter

A multiplier is used to provide a reference V_{xy} which is proportional to the error signal V_e and which has a modulating signal with the desired shape for the input current. Depending on the topology of the PFC stage, it may be beneficial to use as a modulating signal the difference between the input voltage and the output voltage. The control circuit can be simplified by eliminating the multiplier and the sensing of the line voltage. In this case the modulating signal is $V_{xy} = V_e$ and it is essentially constant over the line cycle, because V_e is the control signal from the low-bandwidth output voltage controller. Therefore, the input current is clamped to a value proportional with V_e and its shape approaches a square waveform.

There are several ways to implement the high-bandwidth inner loop. The various current control strategies for implementing the closed loop are:

1. Peak current control
2. Average current control
3. Hysteresis control

(E) AVERAGE CURRENT CONTROL

This technique allows a better input current waveform than the peak current control method as a Current error amplifier (CEA) is introduced in this technique. Average Current control technique is also a two loop control method; it has as an inner current control loop and an outer voltage control loop. This CEA output which is the difference between the average inductor current and the voltage error provided by the outer loop is then compared with a large amplitude ramp waveform with the converter switching frequency using Pulse Width Modulation (PWM) comparator. Thus, the average of inductor current is taken as the reference and the inductor current is forced to follow it. The switch is turned on whenever the inductor current reaches zero and switch is turned off when the inductor current falls below the reference. The voltage Error Amplifier forces the converter output voltage to track the voltage reference by controlling the average inductor current.

The closed loop for the BIZ is implemented as follows: It is a two loop control method, the inner loop being the current control loop and the outer loop being the voltage control loop. Output voltage is sensed and compared with Voltage Reference to generate voltage error. This voltage error is multiplied with input sinusoidal reference current to generate the current reference for the inner loop. This value is compared with input current and the error is given to the PWM generator.PWM generator generates triggering pulses for the switches according to the error.

(F) SIMULATION RESULTS

The various waveforms obtained during the simulation of bridgeless isolated zeta converter in open loop mode using MATLAB/SIMULINK are shown in Figs.11 & 12. The FFT analysis of the converter is done and the results showing the total harmonic distortion in the supply current are obtained.

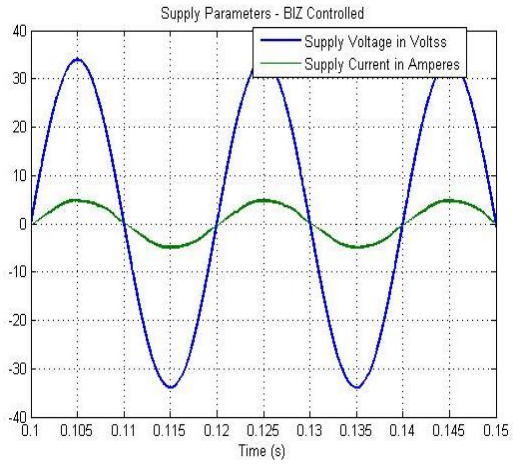

Fig 11. Supply voltage and current waveforms

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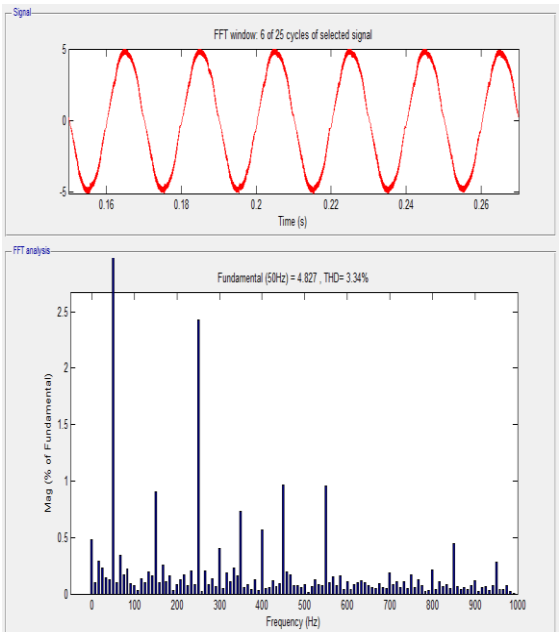

Fig.12 FFT analysis of BIZ in closed loop

From the FFT analysis, the total harmonic distortion (THD) in the supply current is found to be 3.34 %.

IV.PERFORMANCE PARAMETERS

The performance parameters like Total Harmonic Distortion (THD) in the line current, Input Power Factor, Purity Factor, Displacement Factor, Energy Factor and Crest Factor for the Bridgeless Isolated Zeta Converter are defined as follows[15-16]:

(G)TOTAL HARMONIC DISTORTION (THD)

Total Harmonic Distortion of input current is defined as the measure of harmonic content present in the input current. It gives the measure of distortion in the input current waveform when compared with the desired waveform. Mathematically it is defined as follows,

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I^2_{n,rms}}}{I_{1,rms}} \quad (10)$$

where, $I_{n,rms}$ - RMS value of nth harmonic component of the input current, $2 < n < \infty$,
$I_{1,rms}$ - RMS value of the fundamental component of the input current.

(H) POWER FACTOR (PF)

For purely sinusoidal voltage and current, the classical definition is obtained as:

$$PF = \cos \Phi \quad (11)$$

where, $\cos \Phi$ is the displacement factor of the voltage and current.

The line current is non-sinusoidal when the load is nonlinear. For sinusoidal voltage and non-sinusoidal current the power factor can be expressed as

$$PF = K_d \times K_p \quad (12)$$

where, K_d - Displacement factor, K_p- Purity factor.

Hence, the power factor depends on both harmonic content and displacement factor.

(I) DISPLACEMENT FACTOR (K_d)

Displacement Factor of the input current is the measure of the angular displacement between the input voltage and current waveforms. Mathematically, it is defined as follows,

$$K_d = \cos\Phi \quad (13)$$

where, Φ is the angular displacement between input voltage and current waveforms.

(K) PURITY FACTOR (K_p)

Purity Factor or Distortion Factor of the input current describes the harmonic content of the current with respect to the fundamental component. Mathematically, it is defined as follows

$$K_p = \frac{I_{1,rms}}{I_{rms}} \quad , K_p \in [0,1] \quad (14)$$

where, I_{rms} = rms value of the input current with harmonics

The relation between K_p and THD is given by,

$$K_p = \frac{1}{\sqrt{1+THD^2}} \quad (15)$$

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(I) CREST FACTOR

Crest factor describes the ability of an AC power source to generate current or voltage at a particular level. Crest factor is the ratio between the peak value of a waveform to its root mean square (RMS) value.

$$CF = \frac{PK}{RMS} \quad (16)$$

where, CF - Crest Factor, PK - Peak value in volts or amps and RMS - Root Mean Square in volts or amps.

If an electrical signal is a pure sinusoidal wave, the peak value for voltage or current is1.414 times the RMS value. So the crest factor for a pure sinusoid is 1.414.However, the reality is that most generated signals are not perfect in nature. Interactions between the supply and load (with all components in between) will cause distortions to signals and thus affect the relationship between the peak and RMS values. Hence the ratio of peak to RMS value of a waveform will not be exactly equal to 1.414.The crest factor indicates the amount of peaks in an waveform. Higher the crest factor, the no of peaks will be more in the waveform which indicates a distorted waveform. Hence, lesser the crest factor, less distorted is the waveform.

(J) ENERGY FACTOR

During the operation of the DC-DC converter, a portion of energy absorbed from the front end power supply is stored in the converter during the on state of the switching devices and is delivered to the load during off-state.

Energy Factor is defined as the ratio of average stored energy to the output energy in one cycle. Mathematically, it is defined as follows:

$$F_E = \frac{E_S}{V_O I_O T_S} \quad (17)$$

where,F_E - Energy Factor,V_o - Output Voltage I_o - Output Current and T_s - Switching Period.

The energy storage components that can store energy in a PFC switching converter are inductors, capacitors and transformer. During the operation of the converter, these components absorb and deliver energy periodically.

Energy factor for Zeta converter in terms of duty ratio is given as,

$$F_E = 1 + D + (1-D) / (2*k) \quad (18)$$

where, k is a constant determined by the parameters of the circuit which is given as

$$k = 2L_O / (RT_S) \quad (19)$$

where, L_o - Output inductance.

Higher energy factor indicates that the energy stored during the on state is more than the energy delivered to the load during the off-state. High energy factor thus can cause extra losses to the converter such as core loss of inductor, ripple losses on capacitors. Hence, the energy factor should be less in order to reduce the losses. The performance parameters for the proposed zeta converter is compared with the other two topologies a shown in table-3.

Table:3 Comparison of Performance Parameters of all the Zeta Converter Topologies

Parameters	Conventional Zeta	Interleaved Zeta	Bridgeless Isolated Zeta
Total Harmonic Distortion	28.07 %	10.84 %	7.32 %
Power Factor	0.96	0.99	0.997
Energy Factor	1.7	1.7	1.7
Crest Factor	1.619	1.408	1.432

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The performance parameters are evaluated for both open and closed loop configurations of Bridgeless Zeta Converter and are tabulated as shown in Table -4.

Table: 4. Comparison of Open Loop and Closed Loop BIZ PFC

Parameters	Bridgeless Isolated Zeta (Open Loop)	Bridgeless Isolated Zeta (Closed Loop)
Total Harmonic Distortion	7.32 %	3.34 %
Power Factor	0.997	0.9992
Energy Factor	1.7	1.7
Crest Factor	1.432	1.345

V.PROTOTYPE IMPLEMENTATION OF BRIDGELESS ISOLATED ZETACONVERTER

The Hardware Implementation of the Bridgeless Isolated Zeta converter consists of two stages: a) Implementation of triggering circuit for MOSFETS and b) Implementation of Power Circuit.

The gating pulses for the MOSFETS are generated using the code from the Arduino Uno Board with appropriate delay between the pulses. The Arduino Uno board is programmed to produce pulses at an amplitude of 10V with a frequency of 20kHz and 74% duty-cycle. The output from the Arduino Uno Board is given as the input to the Optocoupler circuit inorder to provide isolation between the Arduino Uno board and the power circuit.

The output pulses from the Arduino Uno board are fed into the optocoupler circuit board as shown in Figs.13&14.MCT2E optocoupler manufactured by Texas Instruments is used to couple the pulses from the Arduino Uno board to the MOSFETs. The power supply for MCT2E IC is made possible with the help of bridge rectifier and a regulator. The output of the optocoupler is fed to the gate terminals of the MOSFETs.

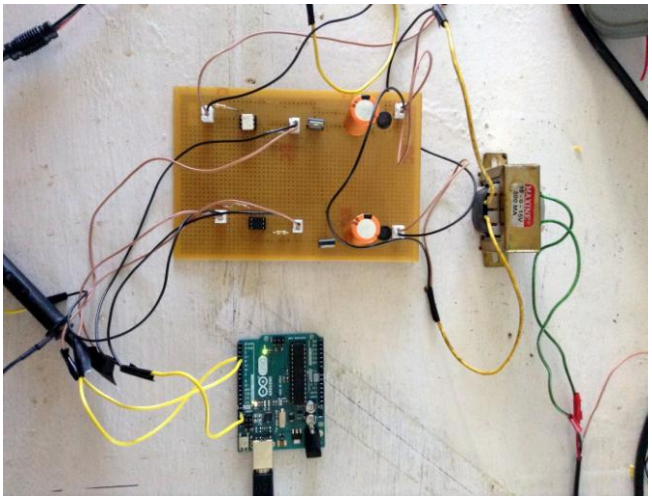

Fig.13 Optocoupler circuit

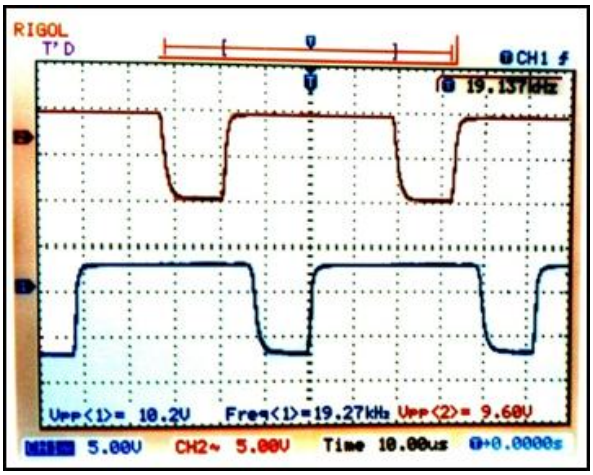

Fig.14 Gating Pulses for MOSFETS

A 24V - 0V - 24V, 5A step down transformer is used to step down the 230V AC supply from the mains to 24V for feeding the converter. A LC EMI filter of specifications 2mH and 2µF is used at the input side for filtering the noise. The power circuit of the converter ass hown in Fig.14 consists of a 1:1:1 high frequency transformer for input-output isolation, two MOSFETs – IRF460, manufactured by Vishay Intertechnology, Inc., Malvern, PA, United States. The MOSFETsare triggered using an Arduino Uno Board which is isolated from the power circuit using an Optocoupler MCT2E, manufactured by Texas Instruments,Dallas,United States. The secondary

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side of the high frequency transformer consists of a 1mF capacitor and a 4mH output inductor connected in series along with a free wheeling diode FR107. A filter capacitor of 5000µF is used to filter out the AC content in the output voltage and a 33 Ohm, 10 Watt resistor is used as the load resistance.

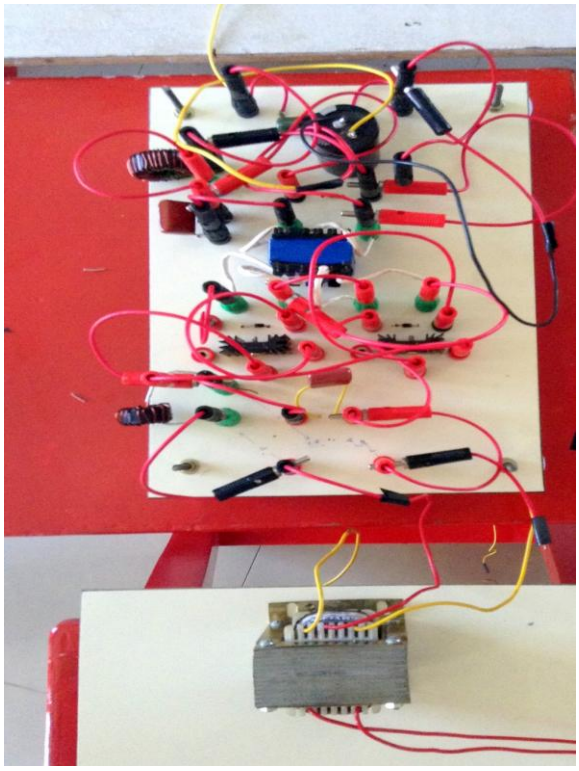

Fig.15 Power Circuit

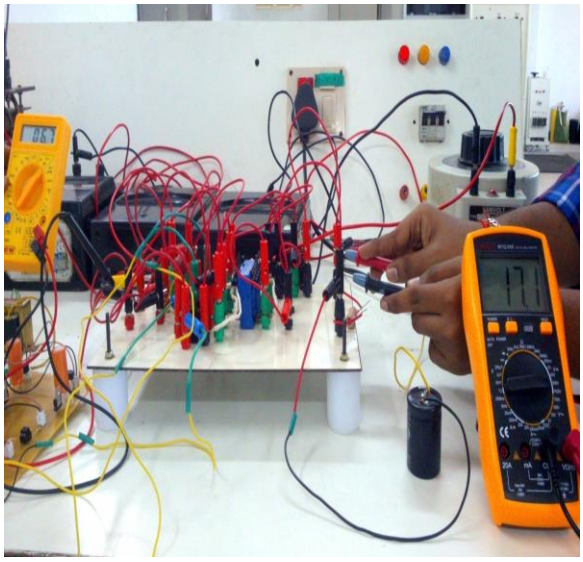

Fig. 16. Output Voltage of the working topology

Fig.17 Power Factor of the Supply Current measured by PQ Analyzer

Fig.16 shows that for an input of 6.7V, an output of 17.1V is obtained which confirms the design and simulation results. In Fig.17, using PQ analyser, the supply power factor obtained is about 0.886 which shows that the proposed zeta converter provides an improved power factor compared to the conventional zeta converter topologies.

VI. CONCLUSION

This paper highlights the advantages of a Zeta topology in power factor correction over the conventional topologies. It also provides a delineated record on the design of a Bridgeless Isolated Zeta Converter with an EMI filter at the supply end as a proposed solution for improving the power factor at the charging end of the HEVs. An average current controller with feedback and feed-forward loops is designed and performance of the closed loop Bridgeless Isolated Zeta converter is analysed. This controller senses the fluctuations at both the supply and the load ends and the error signal thus generated after comparison with the reference value is pulse width modulated to generate a train of pulses for triggering the MOSFETs. Various performance parameters like the Total Harmonic Distortion of the supply current, Supply end Power Factor, Energy Factor, Crest Factor are calculated for the BIZ topology and a comparison of these

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parameters is carried out with the other PFC topologies. Bridgeless Isolated Topology, with its low THD, low voltage ripple and isolation between the Input and the output is considered for hardware implementation.

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