

## A Comparative Analysis of Bridgeless Power Factor Correction (Pfc) Ac-Dc Converter Topologies For Battery Charging Applications

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**Abstract:** The power architecture for the battery charging application includes an AC-DC converter with power factor correction (PFC) followed by an isolated DC-DC converter. In this, AC-DC converter involves a number of non-linear devices which reduces the system power factor and introduce harmonics in the power system leading to undesirable effects. Therefore, it is important to use a suitable power factor correction technique to condition the supply current, and to attain unity power factor. In this paper, a review of bridgeless PFC boost rectifier topologies are discussed and a new dual boost PFC rectifier is proposed. Performance comparison between the conventional PFC boost rectifier and the various types of bridgeless PFC family is performed. Among the various PFC topologies the proposed active DC-DC dual boost PFC circuit gives better efficiency, low THD, and power factor closer to unity. Simulation results and efficiency evaluation in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operations are performed in MATLAB SIMULINK. It was observed that the quality of the line current and current THD in the CCM implementation was improved compared to DCM implementation. Simulation studies of the proposed configuration is performed in MATLAB/SIMULINK and the results are verified.

**Keyword:** Dual boost PFC, Current THD, Power Factor, Efficiency.

### I.INTRODUCTION

The AC mains utility supply perfectly is supposed to be free from current harmonics and high voltage spikes. Discontinuous input supply current that exists on the AC mains due to the non-linearity behavior of the rectification process should be shaped to follow the sinusoidal form of supply voltage [1-2]. Typically there are two ways of shaping the input current waveform one is passive power factor correction and another one is active power factor correction. In passive approach, the passive elements are introduced to improve the quality of the supply line current. As the voltage level of power supply increases, the size of PFC components increases. Due to presence and interaction of inductors and capacitors the system resonance

may occur at different frequencies. Active PFC is a power electronic circuit designed to control the amount of power drawn by a load and obtains a power factor as close as to unity. Normally any active PFC design function is controlling the input current in order to make the current waveform follow the supply voltage waveform closely (i.e. a sine wave). In this, a combination of the reactive elements and some active switches increase the effectiveness of the line current shaping to obtain a controllable output voltage. By this approach automatic correction of the AC input voltage can be obtained [3-4]. This paper presents the design and implementation of one such active PFC AC-DC converter topology, which results in a better supply power factor, efficiency and reduced line current harmonics [5-7]. In this

paper, various types of bridgeless PFC boost rectifier family which includes Bridgeless PFC boost rectifier with bidirectional switch, Bridgeless PFC boost rectifier with two dc/dc boost circuit and conventional/bridge PFC boost converters are discussed[8-9]. Bridgeless PFC rectifiers have been designed for 220 V<sub>ac</sub> input voltage and output voltage of PFC normally regulated to 380V. A comparative evaluation for all the topologies are presented in terms of efficiency, current Total Harmonic Distortion (THD), power factor (PF) and Distortion Factor (DF). Simulations of the all four topology configurations are performed in MATLAB/SIMULINK. Fig.1 shows the current waveform with and without PFC.

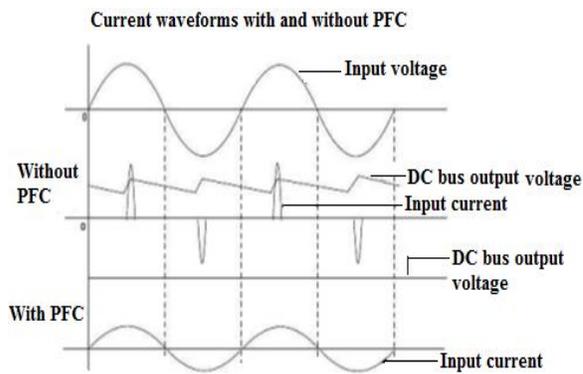


Fig.1 Comparison of current waveform with and without PFC

## II. TOPOLOGIES FOR ACTIVE PFC

In most of the applications, the active PFC controls the input current so that the current waveform is proportional to the nature of the mains supply voltage, a pure sinusoidal wave. Different topologies of active PFC are discussed in the literature[10-12]. This paper discusses on the conventional/Bridge PFC boost rectifier, Bridgeless PFC boost rectifier, Bridgeless PFC boost rectifier with bidirectional switch, Bridgeless PFC boost rectifier with two dc/dc boost converter configuration for shaping the supply current waveform.

### Conventional/Bridge PFC boost rectifier:

The conventional boost converter is the most popular PFC topology because of its simple power circuitry and control design arising from its single-switch construction [13-15]. It consists of a full-bridge diode rectifier followed by the boost converter as shown in Fig.2(a). The diode bridge rectifier is used to rectify the AC input voltage to DC, which is then given to the boost section. When the switch  $S_B$  is in on condition, the DC source energizes the inductor  $L_B$ . In the meantime, the capacitor  $C_B$  maintains the output voltage using the previously stored power. When the switch  $S_B$  is in open condition, both the DC source and the energy stored in the inductor will supply power to the load, hence boosting the output voltage. In this topology Output voltage only depends upon the input voltage and duty cycle as shown in equation 1. By calculating the duty ratio suitably, a desired value of output voltage, higher than the input voltage can be obtained. In this circuit, output ground is always connected to the ac source through the full-bridge rectifier slow-recovery diodes  $D_3$  and  $D_4$ , it has relatively less common mode noise than the bridgeless PFC boost rectifier. In this configuration every moment inductor current goes through three semiconductor devices. It creates degradation of efficiency due to diode bridge rectifier conduction loss. Main disadvantage of this topology is high input current ripple. The design equations of the conventional boost converter are as follows:

The duty ratio (D) of a boost converter is given by

$$\frac{V_O}{V_i} = \frac{1}{1-D} \quad (1)$$

The inductor can be designed using equation

$$L = \frac{R \cdot D \cdot (1-D)^2}{2f} \quad (2)$$

Where  $f$  = switching frequency and  $R$  = Load resistance. The value of capacitance is given by the equation 3

$$C = \frac{V_0 D}{f \cdot \Delta V \cdot R} \quad (3)$$

Where  $\Delta V$  = Output voltage ripple

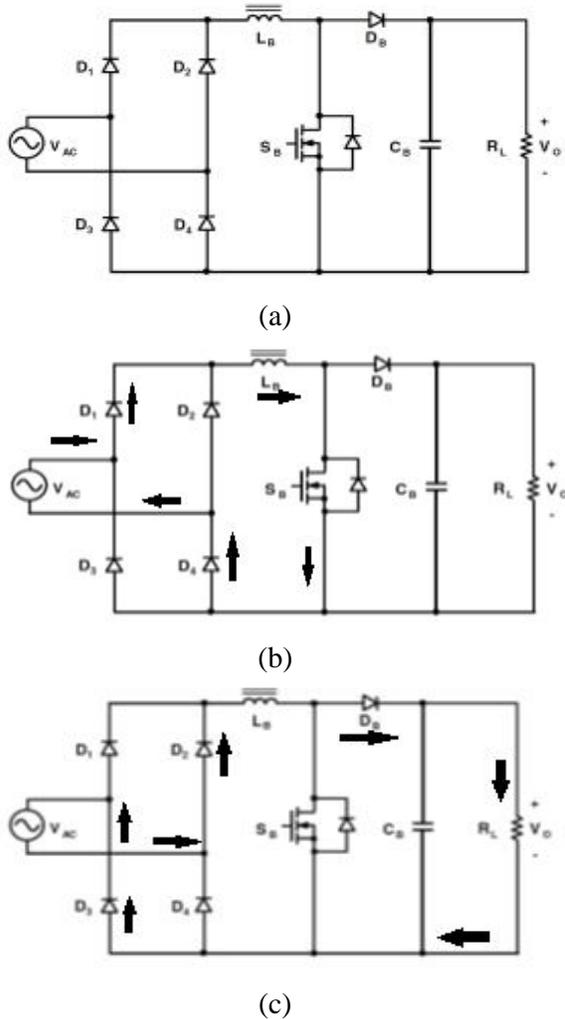


Fig. 2(a) Conventional/Bridge PFC boost rectifier (b)  $S_B$  ON condition (c)  $S_B$  OFF Condition

**Bridgeless PFC boost rectifier:**

The topology of the bridgeless PFC boost rectifier is shown in Fig.3 (a). Compared to the conventional PFC boost rectifier, one diode is removed from the line-current path, so that the line current simultaneously flows through only two semiconductors, resulting in reduced conduction losses. The boost inductor is split and located at the AC side to construct the boost structure [16-17]. The power MOSFET intrinsic body diodes are used to

replace two slow diodes and provide the return path. Switches  $S_1$  and  $S_2$  can be driven with the same PWM signal, which greatly simplifies the control circuit. This topology is not only beneficial in reducing the number of semiconductor switches and conduction loss, but also solves the heat dissipation of the input rectifier bridge problem. When the AC input voltage goes positive as shown in Fig. 3(b), the gate of switch  $S_1$  is driven high and current flows from the input through the inductor  $L_B$ , storing energy. When the switch  $S_1$  turns off, stored energy in the inductor gets discharged and the current flows through diode  $D_1$ , through the load  $R_L$  and returns back through the body diode of switch  $S_2$ . During the negative half cycle of the input signal as shown in Fig.3(c), switch  $S_2$  is operated. When switch  $S_2$  turns on, current flows through the inductor  $L_B$ , and storing energy. When  $S_2$  turns off, energy stored in inductor is released and the current flows through  $D_2$ , through the load  $R_L$  and back to the mains through the body diode of switch  $S_1$ . Thus, in each half line cycle, one of the MOSFET operates as an active switch and the other one operates as a diode. In the conventional boost topology, current flows through two of the bridge diodes in series, whereas, in the bridgeless PFC boost configuration, current flows through only one diode and the return path is provided by power MOSFET. The two slow diodes  $D_3$  and  $D_4$  of the conventional PFC converter are replaced by one MOSFET body diode in bridgeless PFC converter. Thus, the efficiency improvement in bridgeless PFC converter is realized by conduction loss difference between the two slow diodes and the body diode of the MOSFET. However, the implementation of bridgeless PFC boost rectifier is limited by the high common-mode noise problem which caused by the high frequency switches  $S_1$  and  $S_2$ . During the positive half-line cycle, the output ground is always connected to the input ac source through the power switch  $S_2$  body diode, but during the negative half-line cycle, the output ground has high frequency pulsating and the amplitude is equal to output voltage. This

high frequency pulsating voltage source charge and discharge the equivalent parasitic capacitance between the output ground and the ac main line, causing a significantly increased common-mode noise.

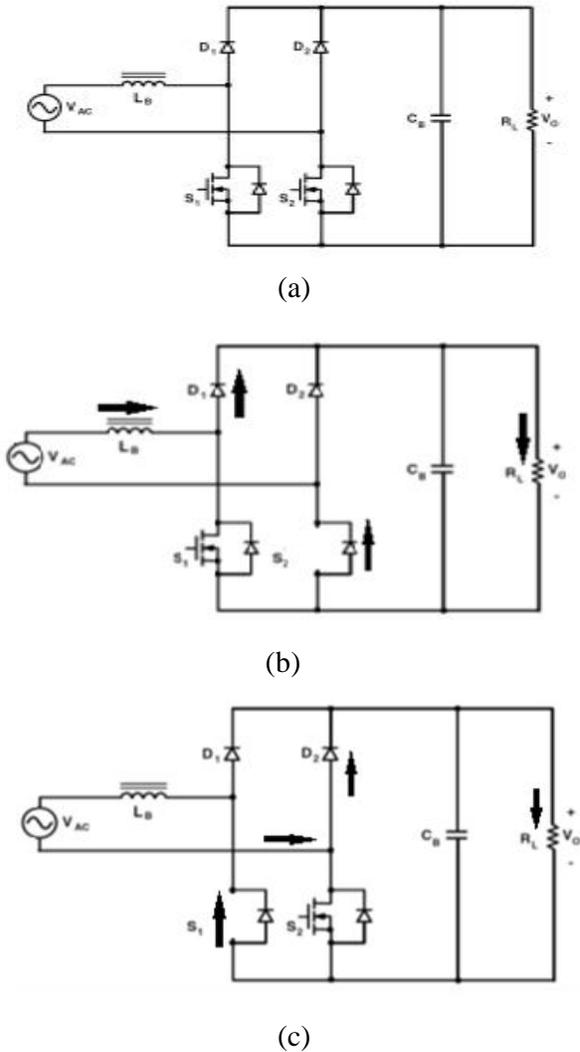


Fig.3 (a) Bridgeless PFC boost rectifier (b) during positive half cycle (c) during negative half cycle

**Bridgeless PFC boost rectifier with bidirectional switch:**

Another modified topology based on the bridgeless PFC boost rectifier is shown in Fig. 4. This topology can also survive from the common-mode noise problem by adding two diodes  $D_3$  and  $D_4$ . Diodes  $D_1$  and  $D_3$  are fast-recovery diodes, whereas diodes  $D_2$  and  $D_4$  are

slow-recovery diodes [18-19]. During the positive half-line cycle, the output ground is connected to the supply ac source through the diode  $D_4$ . During the negative half-line cycle, the positive output bus is connected to the supply ac source through the diode  $D_1$ . So the output voltage is no longer in a floating state, which makes the common mode interference smaller. The major drawback of the topology is that the gate terminal voltage for each switch is different and requires isolated gate drive transformer which makes the drive circuit design difficult. Main difference between Type1 and Type 2 topology is common-source node of switches  $S_1$  and  $S_2$  is disconnected from the output ground. The circuit in Fig.4 (a) can be redrawn as shown in Fig.4 (b), which is the bridgeless PFC boost rectifier with a bidirectional switch. In Type1 or Type 2 topology only two semiconductor devices are in operating state, so the conduction losses are low. In the aspect of sampling the inductor current, complex detection circuit is required. Meanwhile, body diodes of the switches  $S_1$  and  $S_2$  are also in HF switching state. So the topology should not be used in CCM.

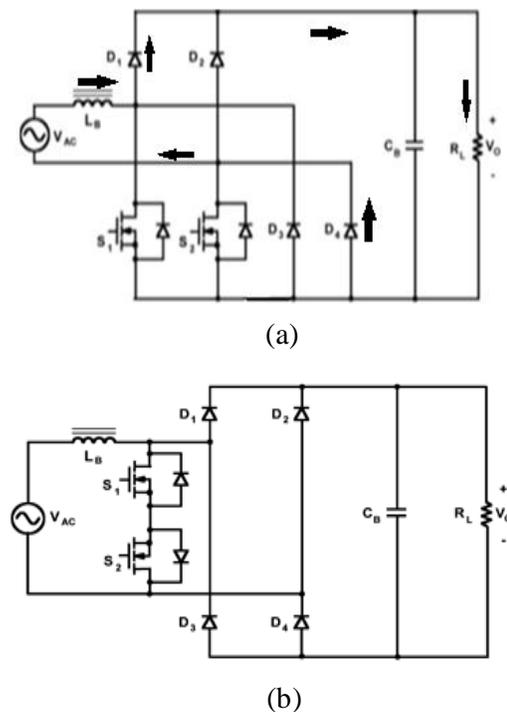


Fig.4 Bridgeless PFC boost rectifier with bidirectional switch (a) Type I (b) Type II

### Bridgeless PFC boost rectifier with two dc/dc dual boost circuit:

To reduce the high common-mode noise, bridgeless PFC boost rectifier is modified by adding two slow diodes and an additional inductor to supply a LF path between the output ground and ac source [20]. This proposed topology consists of two DC/DC boost converter. During the positive half-line cycle of the input voltage, the output ground is connected to the ac source through the slow diode  $D_3$ . During the negative half-line cycle of the input voltage, the output ground is connecting to the ac source through the slow diode  $D_4$ . The symmetric inductors also can be expected as a common-mode filter to reduce the common-mode problem. The proposed bridgeless PFC rectifier topology with two dc/dc boost circuit is shown in Fig.5(a). It consists of two boost PFC rectifiers, each operating during a half line cycle of the input voltage. Inductor  $L_{B1}$  operates during positive half cycle and inductor  $L_{B2}$  operates during negative half cycle. The power Switches  $S_1$  and  $S_2$  it can be driven with the same PWM signal, which significantly simplifies the implementation of control circuit. The operating principle of bridgeless power factor correction boost converter can be divided into four modes. Mode 1 and 2 comes under positive cycle of input voltage and Mode 3 and 4 comes under the negative cycle of input voltage. During the positive half cycle of the input voltage, the first dc/dc boost circuit section,  $L_{B1}$ - $D_1$ - $S_1$  is active through diode  $D_4$ . Diode  $D_4$  connects the ac source to the output ground. The positive half cycle operation can be divided into two modes (Mode 1 and Mode 2). During mode 1 operation as shown in Fig.5 (b), the switch  $S_1$  is in on condition. When the power switch  $S_1$  turns on, inductor  $L_{B1}$  stores energy through the path  $V_{in}$ - $L_{B1}$ - $S_1$ - $D_4$ . During mode 2 operation as shown in Fig.5(c), the switch  $S_1$  is in off condition. When switch  $S_1$  turns off, the stored energy in the inductor  $L_{B1}$  gets released and the current flows through diode  $D_1$ , load  $R_L$ , and returns back to the mains through the diode  $D_4$ . During the negative

half cycle of the input voltage, the second dc/dc boost circuit,  $L_{B2}$ - $D_2$ - $S_2$  is active through diode  $D_3$ . Diode  $D_3$  connects the supply ac source to the output ground. The negative half cycle operation can be divided into two modes (Mode 3 and Mode 4). During mode 3 operation as shown in Fig.5 (d), the switch  $S_2$  is in on condition. When switch  $S_2$  turns on, inductor  $L_{B2}$  stores energy through the path  $V_{in}$ - $L_{B2}$ - $S_2$ - $D_3$ . During mode 4 operation as shown in Fig. 5(e), the switch  $S_2$  is in off condition. When switch  $S_2$  turns off, the energy stored in the second inductor  $L_{B2}$  gets released and the current flows through diode  $D_2$ , load  $R_L$ , and returns to the mains through the diode  $D_3$ . The disadvantage of the bridgeless PFC boost rectifier is that it requires two inductors. On the other hand, it should also be noted that the two inductors compared to a single inductor have better thermal performance. The proposed topology have been designed for 220 V<sub>ac</sub> input voltage and output voltage of PFC normally regulated to 380V DC. It gives the best values for CCM and DCM implementation.

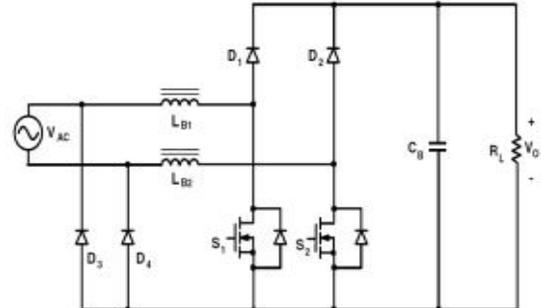
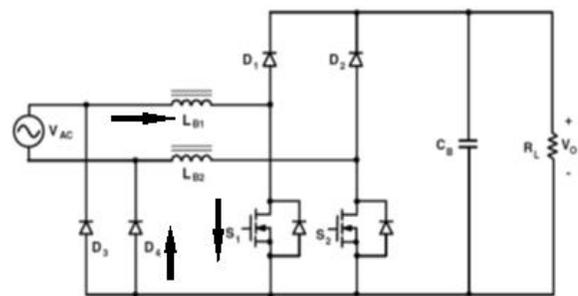
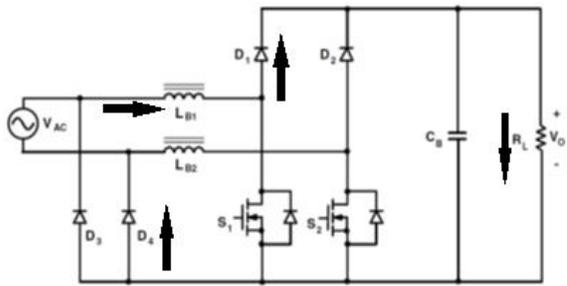


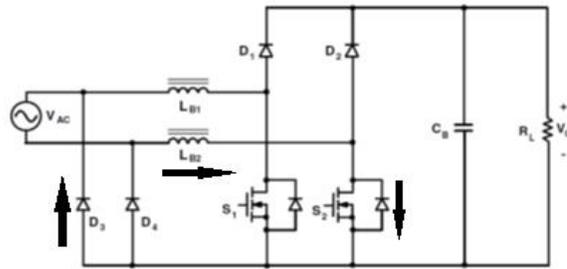
Fig.5 (a) Proposed Bridgeless PFC boost rectifier with two dc/dc dual boost circuit (b)Mode 1 operation (c)Mode 2 operation (d)Mode 3 operation (e)Mode 4 operation



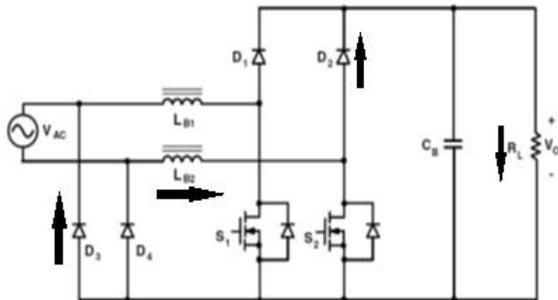
(b)Mode 1 operation



(c) Mode 2 operation



(d) Mode 3 operation



(e) Mode 4 operation

**III MODES OF OPERATION**

Conventional PFC and bridgeless PFC boost rectifier circuits are operated in both DCM (Discontinuous Conduction Mode) and CCM (Continuous Conduction Mode) [21-22]. In these operating modes, we compute the value of power factor, current THD and efficiency.

**Discontinuous Conduction Mode (DCM):**

Discontinuous Conduction mode can be used for switched mode power supply that has power levels of less than 300W. Here the converter’s MOSFET is in ON state when the inductor current reaches the zero value, and turned OFF when the inductor current meets the desired input voltage reference as shown in Fig.6 [23-24]. In this way, the input current

follows that of the input voltage, therefore attaining a power factor close to unity. Compared to continuous mode, this mode requires larger core, higher  $I^2R$  loss and skin effect losses due to the larger inductor current variations. With the increased swing, a larger input filter combination is also required. On the positive side, discontinuous mode switch the boost MOSFET in ON condition when the inductor current is at zero, there is no reverse recovery current ( $I_{rr}$ ) specification required on the boost diode.

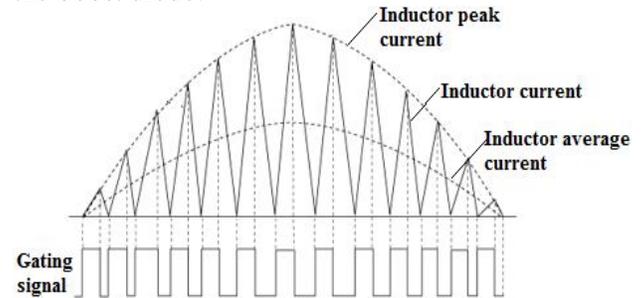


Fig .6 Discontinuous Conduction Mode (DCM)

**Continuous Conduction Mode (CCM):**

Continuous conduction mode can be used for switched mode power supply that has the power levels greater than 300W [25]. Here, converter’s MOSFET does not turn ON when the boost inductor is at zero current, instead of that the current in the energy transfer inductor never reaches zero position during the switching cycle as shown in Fig.7. Because of that, the voltage swing is less in discontinuous mode resulting in lower  $I^2R$  losses and the lower ripple current results in lower inductor core losses. Less voltage swing also reduces the problem of electromagnetic interference and allows for a smaller input filter to be used. Since the MOSFET is not being turned ON when the boost inductor’s current is at zero level, a very fast reverse recovery diode is required to keep losses to a minimum possible.

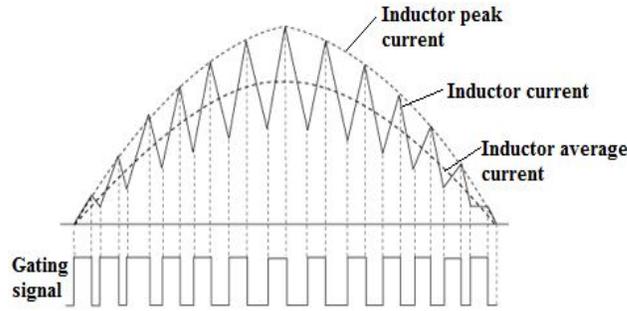


Fig.7 continuous conduction mode

**IV SIMULATION RESULTS**

The various topologies discussed above, namely the conventional/bridge PFC boost rectifier, Bridgeless PFC boost rectifier, Bridgeless PFC boost rectifier with bidirectional switch, Bridgeless PFC boost rectifier with two dc-dc dual boost circuit has been designed and simulated using MATLAB-SIMULINK. The simulation parameters are  $L=85\mu\text{H}$ ,  $C=270\mu\text{F}$  and Duty cycle=50% switching frequency=110 KHz. MATLAB Implementation of conventional/bridge PFC boost rectifier is shown in Fig.8.

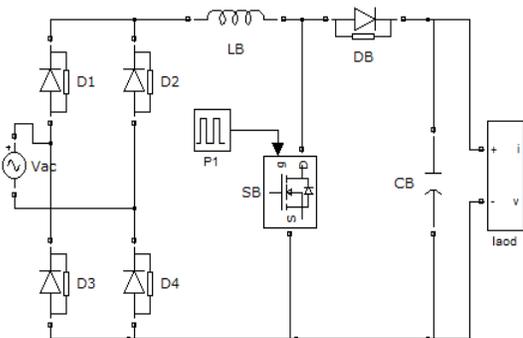
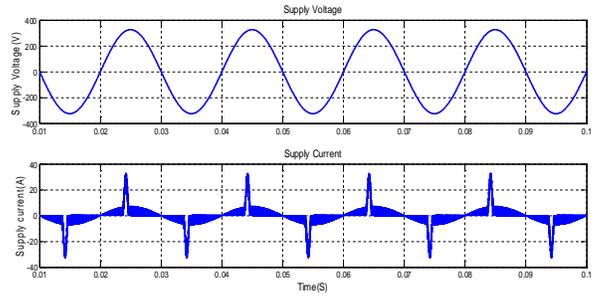
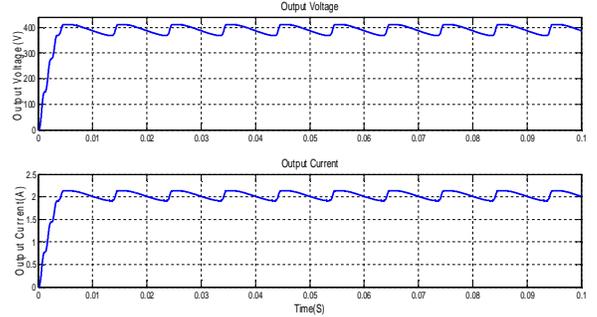


Fig.8 conventional/bridge PFC boost rectifier

Supply Voltage, Supply Current, output voltage and output current waveform of Conventional PFC is shown in Fig.9 (a) & (b)



(a)



(b)

Fig.9 (a) supply voltage & supply current (b) output voltage & output current

FFT analysis of supply current as shown in Fig.10. THD for this circuit is 136.29%

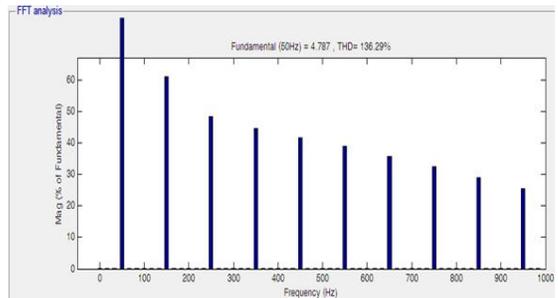


Fig.10 FFT analysis of supply current

MATLAB Implementation of Bridgeless PFC boost rectifier is shown in Fig.11

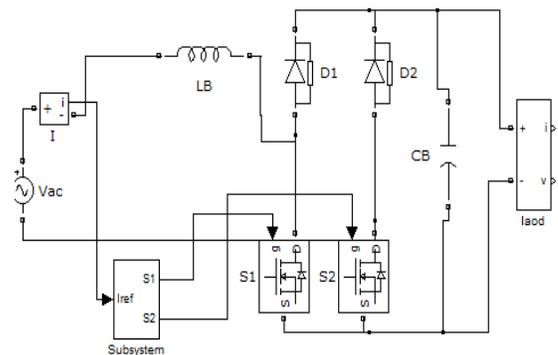


Fig.11 Bridgeless PFC boost rectifier

Supply Voltage, Supply Current, output voltage and output current waveform of Bridgeless PFC boost rectifier is shown in Fig.12 (a) & (b)

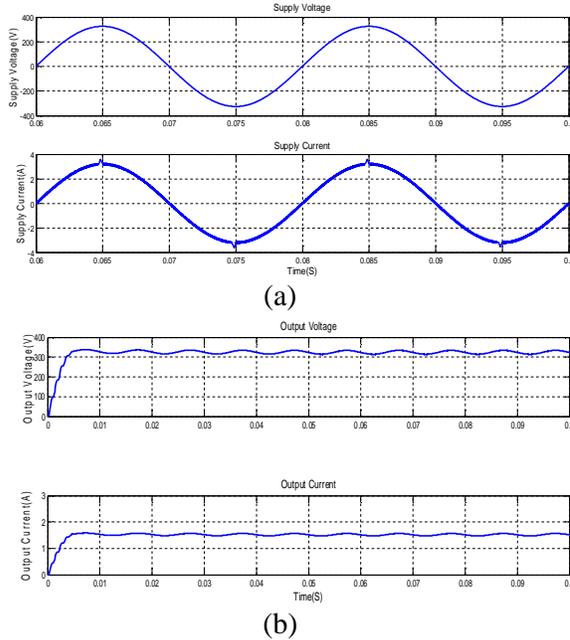


Fig.12 (a) supply voltage & supply current (b) output voltage & output current

FFT analysis of supply current as shown in Fig.13. THD for this circuit is 54.87%

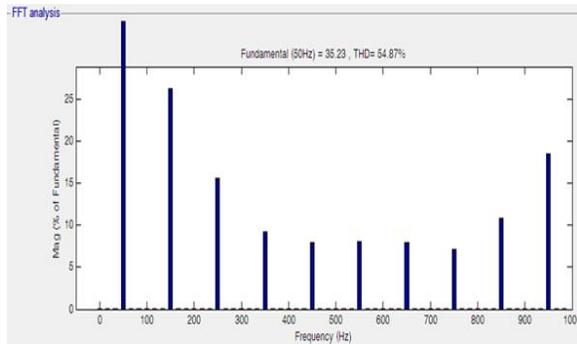


Fig. 13 FFT analysis of supply current

MATLAB Implementation of Bridgeless PFC boost rectifier with bidirectional switch is shown in Fig.14

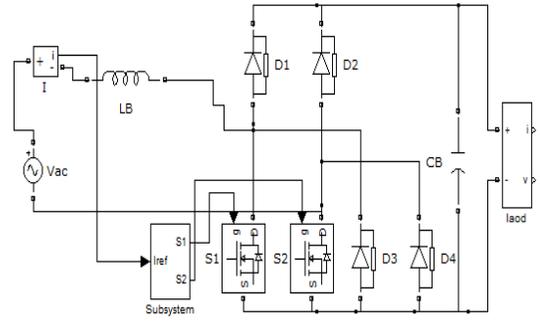


Fig.14 Bridgeless PFC boost rectifier with bidirectional switch

Supply Voltage, Supply Current, output voltage and output current waveform of Bridgeless PFC boost rectifier with bidirectional switch is shown in Fig.15 (a) & (b)

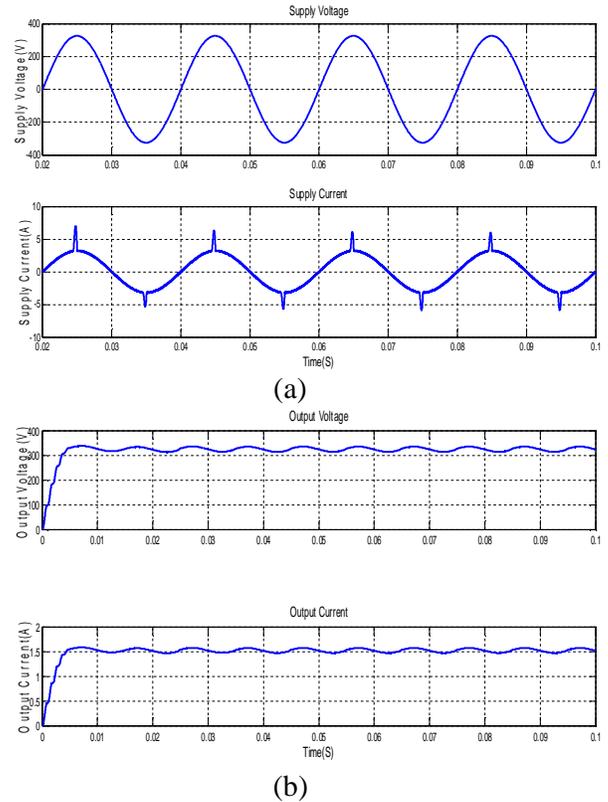


Fig.15 (a) supply voltage & supply current (b) output voltage & output current

FFT analysis of supply current is shown in Fig.16 and THD is about 35.09%

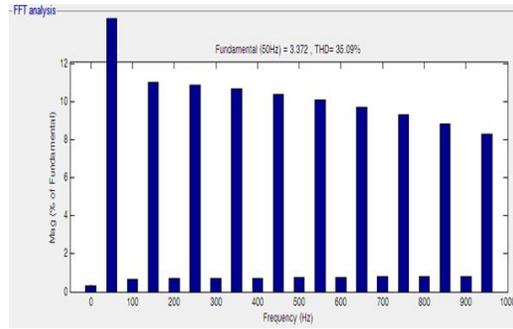


Fig. 16 FFT analysis of supply current

MATLAB Implementation of Bridgeless PFC boost rectifier with two dc-dc dual boost circuit is shown in Fig.17

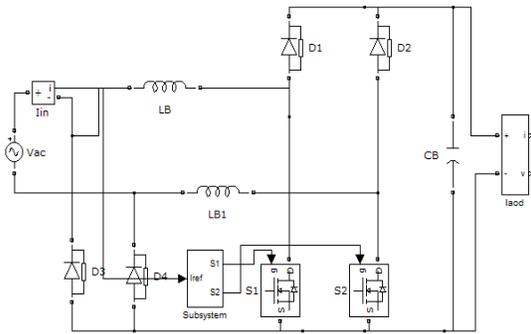
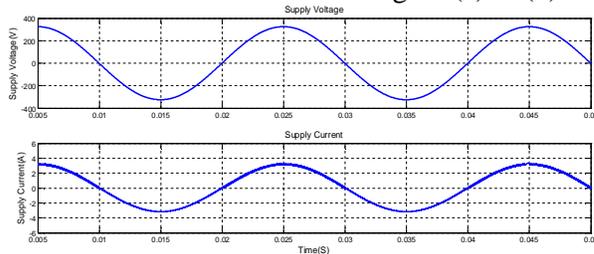
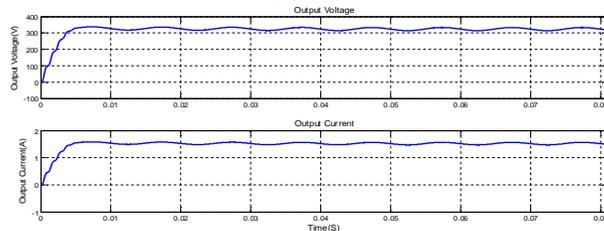


Fig.17 Bridgeless PFC boost rectifier with two dc-dc dual boost circuit

Supply Voltage, Supply Current, output voltage and output current waveform of Bridgeless PFC boost rectifier with two dc-dc dual boost circuit is shown in Fig.18 (a) & (b)



(a)



(b)  
Fig. 18 (a) supply voltage & supply current (b) output voltage & output current  
FFT analysis of supply current is shown in

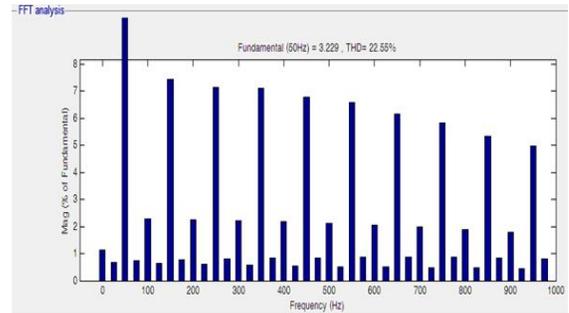


Fig.19 and THD is about 22.55%

Fig.19 FFT analysis of supply current

DCM operation of the proposed DC-DC dual boost PFC is carried out under 10 ohm load. Inductor current & Pulse Pattern is shown in Fig.20. Here the triggering pulses are ON when the inductor current reaches zero. The DCM implementation had a slightly better efficiency 80.51% than the CCM implementation. FFT analysis of supply current under DCM operation is shown in Fig.21. In this case, current THD is higher.

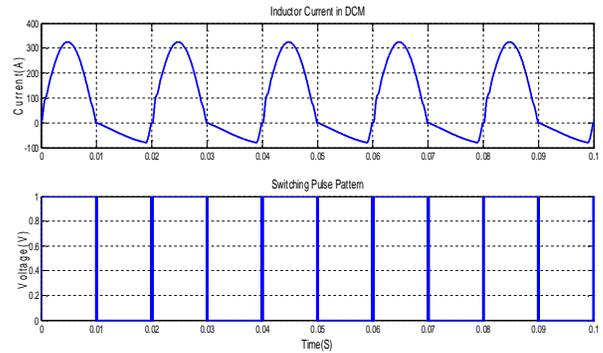


Fig.20 Inductor current and pulse pattern in DCM

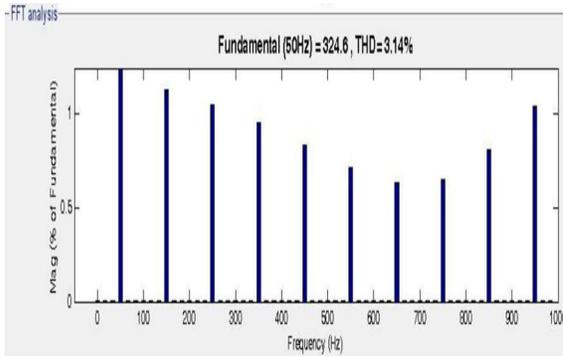


Fig. 21 FFT analysis of supply current under DCM operation

CCM operation of the proposed DC-DC dual boost PFC is carried out under 300ohm load. Inductor current & Pulse Pattern in CCM is shown in Fig.22. Here boost converter's MOSFET does not switch ON when the boost inductor current is zero. FFT analysis of supply current under CCM operation is shown in Fig.23. In this case current THD is 2.88% which is less compared to DCM implementation.

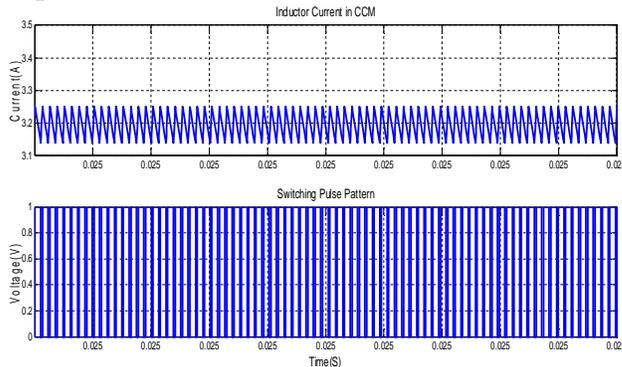


Fig. 22 Inductor current and pulse pattern in CCM

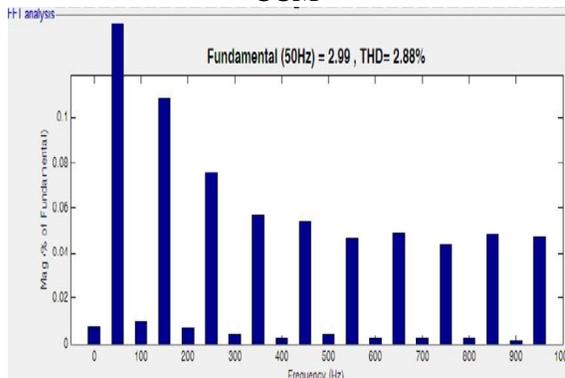


Fig.23 FFT analysis of supply current under CCM operation

V. PERFORMANCE PARAMETERS OF PFC TOPOLOGIES

a) Power factor (PF):

If the voltage and current waveforms are ideal in nature then the  $PF = \cos\phi$ . But for the sinusoidal voltage and non-sinusoidal current, the PF should be equal to [26-27]

$$PF = \frac{V_{rms} \cdot I_{rms1}}{V_{rms} \cdot I_{rms}}$$

$$PF = K_d \cdot \cos\phi$$

$V_{rms}$  = Root Mean Square of supply phase voltage

$I_{rms}$  = Root Mean Square of supply phase current

$I_{rms1}$  = Root Mean Square of fundamental component of the supply current

$\phi$  = phase angle between the supply voltage and fundamental component of the supply current.

$K_d$  is the ratio of the fundamental of line current RMS value to the total line current RMS value.

$$K_d = \frac{I_{rms1}}{\sqrt{I_{rms1}^2 + I_{rms2}^2 + \dots + I_{rmsn}^2}}$$

n is the nth order of harmonic current.

The power factor can be represented as

$$PF = \frac{\cos\phi}{\sqrt{1 + (THD)^2}}$$

From the power factor expression, the reasons leading to poor power factor are line current has large amount of high order harmonic and the different phase between input voltage and current. Therefore, to improve the power factor, the line current should keep the same phase with the sinusoidal line voltage and attenuate the line current harmonics.

b) Distortion factor ( $K_d$ ):

It is a measurement of the non-linearity of the impedance of the input. If there is deviation in the input impedance, which varies as a function of the input voltage, then there will be distortion of the input current and hence,

this distortion will lead to reduced power factor.

$$K_d = \frac{1}{\sqrt{1 + (THD)^2}}$$

c) Total Harmonic Distortion:

It is a measurement of the harmonic distortion occur in a signal and is defined as the ratio of the square root of the sum of the squares of all harmonic components to the fundamental frequency component. THD is an important figure of merit used to calculate the level of harmonics in voltage or current waveforms.

$$THD = \frac{I_h}{I_{rms_1}}$$

$$THD = \frac{\sqrt{I_{rms_2}^2 + I_{rms_3}^2 + \dots + I_{rms_n}^2}}{I_{rms_1}}$$

$I_h$  is the sum of total harmonic current RMS values.

As mentioned above, the proposed topology gives the best performance in comparison to the other topologies, which justifies its choice for implementation purposes. Performance parameters of active power factor topologies as shown in Table I. It is clear that the DC-DC dual boost PFC is better for front end applications because of the following reasons: Power Factor value is closer to unity, High efficiency compared to other topologies, minimum current THD. The Bidirectional PFC also has closer unity Power Factor but this topology has high current THD and low efficiency compared to the proposed DC-DC dual boost PFC topology. Comparison chart of efficiency between Conventional and DC-DC dual boost PFC rectifier circuit as shown in Fig.24. The efficiency is high all at the time in DC-DC dual boost rectifier for various loads.

Table I

Topologies	PF	Current THD	Distortion Factor	Efficiency
Conventional/Bridge PFC boost rectifier	0.9813	136.29	0.0073	55.22
Basic Bridgeless PFC boost rectifier	0.9822	54.87	0.0182	55.71
Bridgeless PFC boost rectifier with Bidirectional switch	0.9835	35.09	0.0284	85.5
DC-DC Dual Boost PFC topology	0.9998	22.55	0.0443	95.49

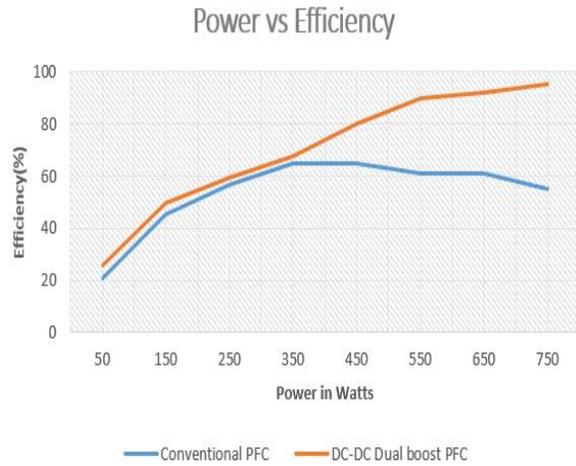


Fig.24 Comparison chart of efficiency between Conventional and DC-DC dual boost PFC rectifier circuit

VI CONCLUSION

This paper has presented a single-phase Bridgeless PFC Boost Converter. Compared to the conventional PFC boost converter, the efficiency of the proposed converter is about 95.49%. Therefore, it is suitable for front end PFC stage by eliminating one line diode forward-voltage drop in the line-current path. The proposed topology was investigated under CCM and DCM conditions. It was found that the quality of the line current in the CCM implementation was better than that of DCM. From the results, it was found that the CCM dual-boost PFC topology has lesser current THD and power factor closer to unity compared to the other bridgeless topologies and it provides a good solution for low cost

high power factor AC–DC converters with fast output regulation.

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