

## A Novel SEPIC Power Factor Correction Converter for HBLED Applications

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**Abstract :** In LED applications, high power factor and low harmonics are of utmost importance. This paper presents a novel single-ended primary inductance power-factor-correction converter (SEPIC PFC) for driving LED lamps with high PFC. The proposed Bridgeless Interleaved SEPIC converter improves the power quality at input AC mains. The design, modeling and simulation are carried out in MATLAB/SIMULINK environment for 12V, 50 Hz AC mains to drive a 10 W LED load at a voltage of 24V. The Loss analysis is also carried out for the proposed converter to calculate its efficiency. A laboratory prototype of the proposed converter to drive load consisting of two 11W LED drivers in series (each with four parallel strings and four 0.8W LEDs in series) is tested to verify the feasibility of the proposed converter. The system performance is evaluated in terms of power quality indices such as total harmonic distortion of AC mains current, power factor and distortion factor.

**Keywords:** LED, Power Factor correction, SEPIC, Bridgeless SEPIC, Interleaved SEPIC

### 1. INTRODUCTION

LED lighting solutions have become the order of the day. The conventional lighting systems featuring incandescent lamps, fluorescent lamps and compact fluorescent lamps are being replaced with LED systems due to their advantages such as:

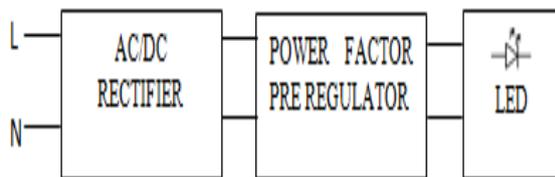
- Low power consumption resulting in energy conservation. This is a significant feature as Lighting applications account for approximately 20 % of electrical energy consumed in the world.
- High efficiency as their efficacy is greater than 25lm/w compared to the conventional light sources.
- Environment-friendly features as they do not contain mercury or they don't generate heat due to Infrared radiation.
- LEDs as such are highly reliable and further reliability is built into the system by having more number of

LED arrays so that total blackout is totally eliminated as even if one of the LEDs fail, the other LEDs will continue functioning.

- One 60 W incandescent bulb with an efficiency of 20 lm/W produce 1200 lumens. Compared to this a single one-watt LED with an efficiency of 30 lm/W produces 30 lumens i.e. 40 such LEDs are required to produce the same amount of light as the incandescent bulb.

In practice, almost all electrical loads are reactive in nature which results in poor power factor leading to inefficient power transfer adversely affecting the power grid currents. LEDs are nonlinear, non-resistive loads giving rise to some unique drive issues which needs to be addressed to achieve unity power factor. The efforts of electrical engineers have always been to render the load reactance to the

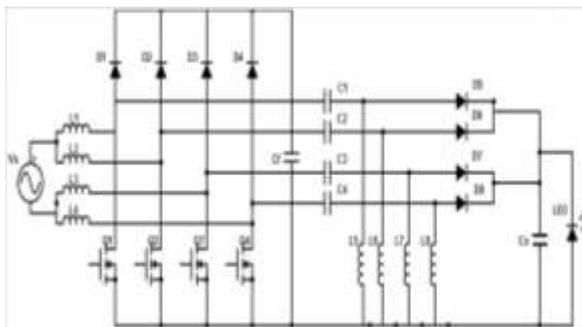
resistance looking into the input source by passive or active means. The aim has always been to attain unity power factor. Significant research is going on in the area of power factor correction to eliminate harmonic contamination and improve the efficiency of the system to achieve maximum power transfer [1]. To meet the international standards of power quality regulations, a modern solution for this problem is incorporation of an active power factor correction block called power factor pre-regulator in the DC-DC converters. By controlling the duty cycle of the active switches, the line current can be shaped so as to be in phase with the supply voltage [1].



**Fig 1.** Basic LED drive schematic

In this paper, a power factor corrected (PFC) SEPIC converter is proposed to drive an array of LEDs (Fig.1). In this topology, the THD of AC mains current achieved is less than 7%. The paper is organized as follows: In Section II, the salient features including the Design equations and Power Loss analysis of the proposed SEPIC converter for driving LED lamp is discussed. The simulation results are presented in Section III. The hardware implementation methodologies are discussed in Section IV. Experimental results to verify the validation of the proposed driver are also presented.

## 2. Bridgeless Interleaved SEPIC Converter



**Fig.2** Bridgeless Interleaved SEPIC converter

The bridgeless Interleaved SEPIC topology combines the benefits of both the bridgeless topology and the interleaved structure[2-5]. The circuit diagram is shown in Fig.2.

- This topology is superior and offers a number of advantages compared to the conventional topologies.
- The prime feature of this topology is that the input diode bridge rectifier stage is integrated with the classic SEPIC topology. So the input diode bridge rectifier stage is eliminated and thus the circuit becomes less bulky.
- The efficiency of the system improves with bridgeless configuration as the high conduction loss caused by the high forward voltage drop of the diode bridge is absent. So the heat management problem caused by the input diode rectifier stage is also solved.
- Interleaving leads to an increase in the frequency of input current ripples and hence a reduction in the weight and volume of EMI filters required.
- The conduction losses are greatly reduced due to the presence of fewer number of semiconductor devices in each conduction path.
- This topology uses two extra MOSFETs and fast diodes, instead of the four slow diodes in the bridge rectifier stage.
- Thus this topology can exhibit maximum efficiency due to the combined merits of interleaving and the bridgeless structure

The circuit operation is divided into two modes. During the positive half cycle,  $Q_1/Q_3$  is turned on and current flows through  $L_1-Q_1$  and  $Q_3-L_3$ , returning to the line and thus energy gets stored in  $L_1$  and  $L_3$ . When  $Q_1/Q_3$  are turned off,  $L_1$  and  $L_3$  releases its stored energy and thus the current flows through  $C_1/C_3$ , through the load and returns through the body diode of  $Q_3$  back to the input mains. The inductors  $L_5/L_7$  connected to switches  $Q_1/Q_3$  take energy from the SEPIC capacitor  $C_1$  and  $C_3$ . The output capacitor supplies the load[5-6]. During the negative half cycle,  $Q_4/Q_2$  is turned on and current flows through  $L_4-Q_4$  and  $Q_2-L_2$ , returning to the line; during this period, energy is stored in  $L_4$  and  $L_2$ . When

$Q_4/Q_2$  are turned off,  $L_4$  and  $L_2$  releases its stored energy and thus current flows through  $C_2/C_4$ , through the load and returns through the body diode of  $Q_2$  back to the input mains. The inductors  $L_4$  and  $L_2$  connected to switches  $Q_4/Q_2$  take energy from the SEPIC capacitor  $C_2$  and  $C_4$ . The output capacitor supplies the load.

### 2.1 Design Equations

The design of SEPIC converter involves the selection of duty cycle, inductor and SEPIC capacitors. The following equations are used for design purpose [7-8].

Selection of Duty cycle, D:

The duty cycle, D is defined as

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} = M \quad (1)$$

where M is conversion ratio,  $V_o$  is Output voltage (V) and  $V_{in}$  is Input Voltage (V).

- Selection of Inductors:

The value of the Inductor decides the mode of operation i.e. Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM).

For CCM mode,  $L_{1c} > L_{1c} ; L_{2c} > L_{2c}$

$$L_{1c} \geq \frac{R_L}{2f_{sw}(M+M^2)} \quad (2)$$

$$L_{2c} \geq \frac{R_L}{2f_{sw}(M+1)} \quad (3)$$

where  $f_{sw}$  is Switching Frequency (kHz).

The design of Inductor values is very critical as it directly varies the voltage conversion ratio. The inductors values are designed such that its ratio follows equation (4).

$$\frac{L_2}{L_1} = M \quad (4)$$

- Selection of Output Capacitor:

The output capacitor  $C_o$  must have enough capacitance to maintain constant DC link voltage with less ripple and must have to provide continuous load current at high switching frequency.

$$C_o \geq \frac{P_o}{4\omega\Delta V_o} \quad (5)$$

where  $P_o$  is output power (W) and  $\Delta V_o$  is change in output voltage.

### 2.2 LED Modeling

For an LED to conduct current and emit light, the applied voltage across the LED must be greater than the cut-in voltage. One approximate linear model of an LED is a series combination of the following components: an internal resistance ( $R_{LED1}$ ) and an ideal diode with a cut-in voltage [9-12]. A real LED can be represented by the equivalent circuit as shown in Fig.3 consisting of an ideal diode in series with resistance  $R_{di}$ . The LED load current-voltage model would be the following:

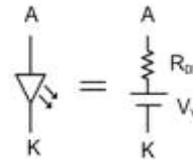


Fig.3 LED equivalent model

The device voltage  $V_d$  is

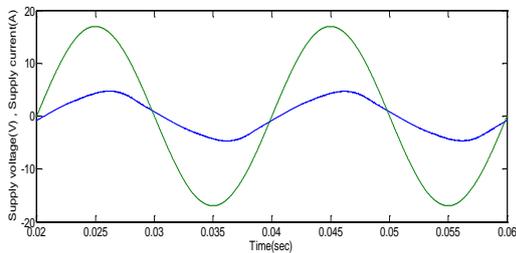
$$V_D = I_D R_D + V_\gamma \quad (6)$$

where  $V_D$  is the forward voltage drop of the LED,  $R_D$  is the dynamic resistance,  $I_D$  is the LED forward current and  $V_\gamma$  is the threshold voltage. The LED used here is High Brightness LED (HB-LED). As the number of LEDs are more, they dissipate more heat and are thus placed over a heat sink. The parameters of HB-LED are:  $V_{LED}=12V$ ,  $I_{LED}=800mA$ , Rated Power=10W, CRI=80%. The number of LEDs used here is 8 parallel strings with 8 LEDs in series.

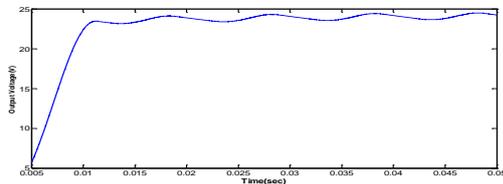
### 3. Simulation Results

A MATLAB model of the proposed PFC SEPIC LED driver is developed to study the performance with reference to the power quality issues. The simulation circuit for the bridgeless interleaved SEPIC converter is shown in Fig.2. Calculated values of components of PFC SEPIC converter acquired from various design equations are selected appropriately to achieve desired power quality at AC mains. The simulation parameters are chosen based on the design equations discussed. The design parameters are: input

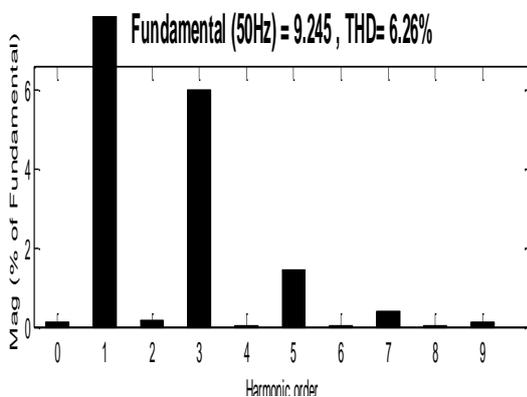
voltage=12V, Switching Frequency=25kHz , Duty Cycle=59% , L1 , L2 , L3 , L4=2.8mH, L5 , L6 , L7 , L8=4.03mH, C1 , C2 ,C3,C4=10μF, Output Capacitor=3200μF , Output voltage=24V.



(a)



(b)



(c)

**Fig.4.** (a) Supply voltage and supply current (b)Output voltage (c)FFT analysis of Bridgeless Interleaved SEPIC converter

The simulation results for bridgeless Interleaved SEPIC converter are shown in Fig.4. From Fig.4a, it is obvious that the input line current almost faithfully follows the input line voltage in sinusoidal manner. Fig 4b shows the output voltage waveform. Fig.4c shows the line current harmonic spectrum and the calculated value for power factor is 0.9882.

**Table 1. Comparison of performance parameters of SEPIC converter**

SEPIC Converter Topology	THD (%)	$K_d$	$K_0$	Power Factor
SEPIC converter	16.79	0.9862	0.9855	0.9719
Bridgeless SEPIC converter	9.35	0.9956	0.9855	0.9738
Interleaved SEPIC converter	11.43	0.9902	0.9935	0.9838
Bridgeless Interleaved SEPIC converter	3.90	0.9992	0.9956	0.9950

The proposed SEPIC topology is compared with conventional SEPIC, Bridgeless SEPIC, Interleaved SEPIC converters through MATLAB simulation and the performance parameters are tabulated in Table 1. The performance parameters obtained show that the bridgeless Interleaved SEPIC topology offers optimal power factor compared to conventional SEPIC topologies.

**4. Hardware Implementation**

To experimentally validate the proposed SEPIC topology, a prototype is developed. The hardware setup comprises of main power circuit and MOSFET gate driver pulse generation. The load of the converter is a series of HB-LEDs.

**Table 2. Hardware components for Pulse Generation**

Components	Specification
Transformer	230 V/15 V, 1A
Diode Bridge Rectifier	W10
Voltage Regulator	7815
Electrolytic Capacitor	1000μF, 63 V
IC555	NE555
Optocoupler	MCT2E
CMOS NOT Gate	IC4069

#### 4.1. Implementation of gating circuit.

The gating pulses are generated using 555 timer to trigger the MOSFETs of the power circuit. 555 timer when operated in astable mode generates a continuous stream of square pulses at a specified frequency[13-14]. To generate pulses with switching frequency of 25 kHz and pulse width of 59%, Resistor  $R_1=2.2k\Omega$  is connected between  $V_{CC}$  and the discharge pin (pin 7) and another resistor  $R_2=1.1k\Omega$  is connected between the discharge pin (pin 7) and the trigger (pin 2) and threshold (pin 6) pins that share a common node. The gating circuit is isolated from the power circuit using the MCT2E optocoupler. The output of the optocoupler [14] is then given to the Power MOSFETs across gate and source. Two of the switches in the proposed topology are triggered at a frequency of 25 kHz (0.04 ms) while the other two switches are triggered at the same frequency, but with a phase lag of 180 degrees using CMOS NOT gates. Fig 5 shows the generated pulses of frequency 25 kHz with Duty cycle of 59%.The pulses are phase shifted by  $180^\circ$ .The experimental setup is shown in Fig 6. It consists of a power supply stage for deriving 12V from 230V mains input, a clock circuit using 555 timer for generating 25 kHz clock pulses, phase conversion circuit using NOT gate, isolation circuit using optocoupler, and HB-LED lighting load.

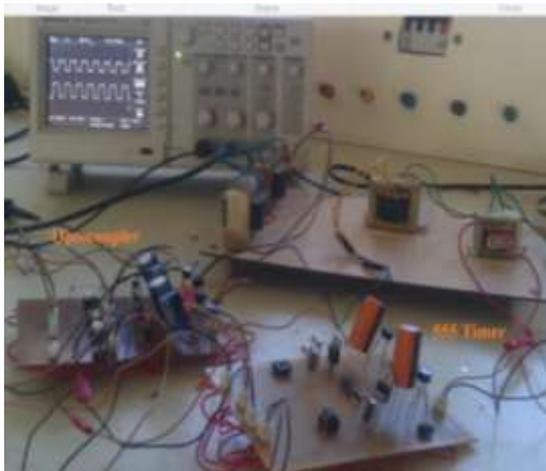


Fig 5. Pulses generated using 555 timer IC

To confirm the simulation results, a laboratory prototype is constructed to the following specification: • Input Voltage: 12V, switching

Frequency: 25 kHz and rated Output Voltage: 24V.

Table 3. Hardware components for proposed topology

Components	Parameter	Specification
Diodes	D1,D2,D3,D4	IN5418
Diodes	D5,D6,D7,D8	IN4007
Inductors	L1 , L2 , L3 , L4	2.8mH,2A
Diodes	L5 , L6 , L7 , L8	4.03mH,2A
SEPIC Capacitors	C1 , C2 , C3 ,C4	10 $\mu$ F,23V
Output Capacitor	Co	3200 $\mu$ F,63V
MOSFET	Q1,Q2,Q3,Q4	SDP03N60C3

The circuit parameters for the laboratory prototype are summarized in Table 3. The prototype is designed to supply four paralleled LED lamps of 22W with a maximum output current of 1.6A. The experimental results of the Bridgeless Interleaved SEPIC topology are shown in Fig.6 and Fig.7. An output voltage of 21.4V is measured in the multimeter for an input of 12V.The power factor is observed to be 0.936 which is close to simulated result .The output voltage and current waveform obtained in the PQ analyzer is shown in Fig.8.It is observed that the load voltage and current have a nearly DC value with small ripples.



Fig.6. Output voltage of SEPIC Converter for an input of 12V

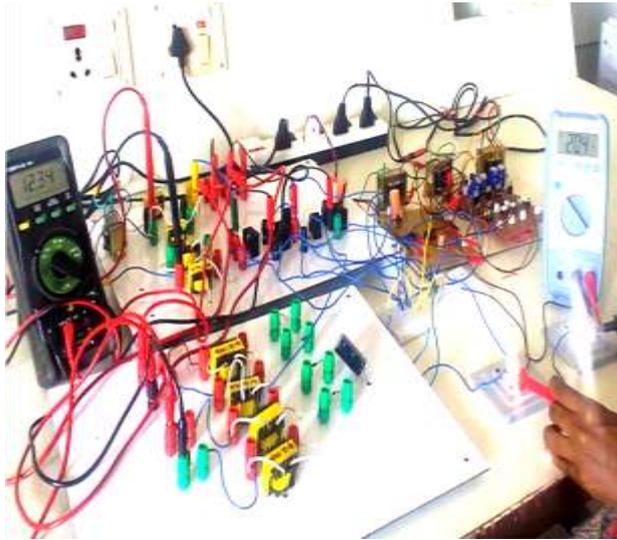
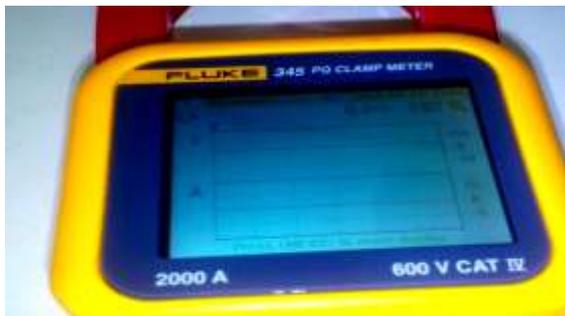


Fig.7. Hardware Circuit of the Proposed AC-DC Converter for PFC



(a)



(b)

Fig 8.(a) PQ Analyser shows the power factor of 0.936(b)Output voltage of 22V and current of 900mA waveforms

To further improve power factor and make it closer to unity, feed forward and feedback loops are introduced in the circuit to detect and shape the supply current and to reduce its harmonic distortion. For the proposed topology, current mode control is implemented and the output is verified. Fig.9 shows the

pulse generation using current mode PWM IC UC3842[13]. Fig.10 shows the hardware circuit for current mode controller.

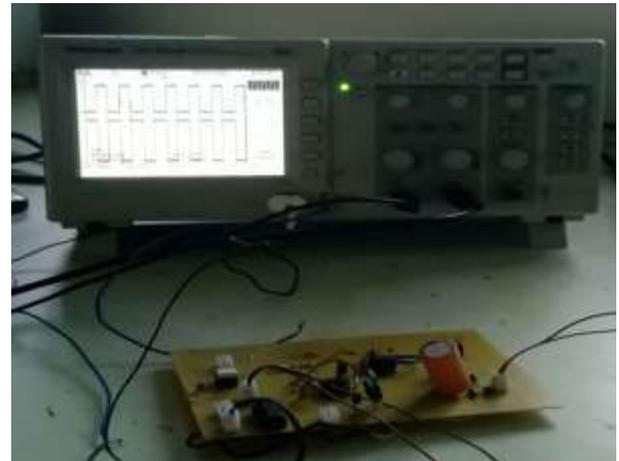


Fig 9. Pulses generated using UC3842 IC

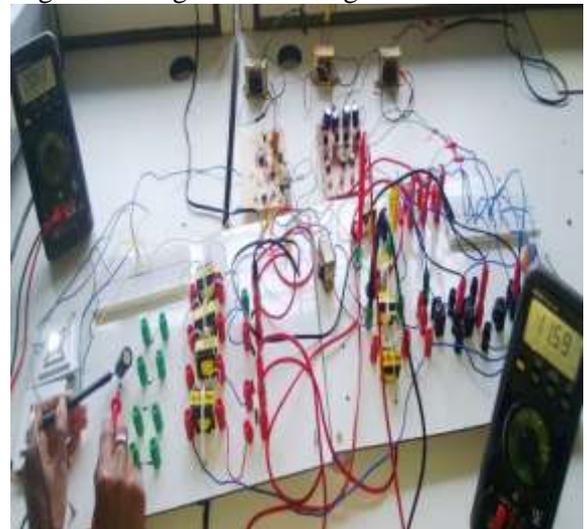


Fig.10 Current mode control for the proposed converter using UC3842

With current mode PWM control, the supply current THD is reduced to 4.80% and the power factor is improved to 0.9936. Therefore, with suitable closed loop current control techniques, the supply factor can be improved.

## 7. CONCLUSION

In this paper, a novel SEPIC power factor correction converter called Bridgeless Interleaved SEPIC converters for LED applications with low line current harmonic distortion and high efficiency has been proposed and verified experimentally. A comparative analysis of the performance parameters of conventional SEPIC converters are made between the proposed converter and

conventional SEPIC converters .A laboratory prototype was built and tested with HB-LED load of 24V, 22W. The measured value of power factor is 0.936 .The experimental results are found to closely match the simulation results.

### ACKNOWLEDGEMENT

The authors wish to express their gratitude to the management of SSN Institutions, Chennai, India for funding this project and providing all the laboratory facilities to carry out this work.

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